A STUDY OF THE INFLUENCE OF TUNNEL OXIDE THICKNESS ON THE PERFORMANCE OF FLASH MEMORY BASED ON ION-BEAM SYNTHESIZED SILICON NANOCRYSTALS

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Silicon nanocrystal-based memory devices have recently attracted much attention due to their potential to overcome the limitations of current poly-silicon based floating-gate memory [1]. The Colomb blockade effect and the energy level quantization of the silicon nanocrystal layer provide the possibilities of long-term charge storage at room temperature and even at hot temperatures [2]. In this paper, we evaluate the performance of the memory devices based on silicon nanocrystal synthesized by Si ion implantation at a very low energy with different tunnel oxide thicknesses.

The MOSFETs containing silicon nanocrystals are fabricated with a conventional CMOS technology. Initially, SiO_2 were thermally grown to either 20 nm (sample 1) or 17 nm (sample 2) on p-type Si wafers. Silicon nanocrystals were synthesized with the ion-beam technique, i.e., Si^+ ions are implanted into the SiO_2 thin film at 2 keV, and then a high temperature annealing at 1000 ^oC in N_2 ambient was carried out. Another 20 nm SiO_2 were then deposited onto the initial SiO_2 to form the control oxide. The size of the silicon nanocrystal is approximately ~4.5 nm as determined from the high-resolution transmission electron microscope (HRTEM) measurement. The tunnel oxide (t_{tunn}) is approximately 7-8 nm and 3-4 nm for sample 1 and sample 2, respectively. Fig. 1 shows the HRTEM cross section of sample 2.

The performance of the memory devices has been evaluated. For the MOSFETs with tunneling-oxide thickness t_{tunn} = 7 nm, Fowler-Nordheim (FN) tunneling mechanism is used for the programming and erasing operations. At room temperature and the hot temperature (85 ^oC), the device exhibits a ~0.5 V threshold voltage window difference under a short write / erase pulse of +12 V / -12 V for 1 ms (FN tunneling mechanism). The device shows good endurance up to 10^5 write / erase cycles. However, the memory window starts to drift up after 10^5 write / erase cycles as shown in Fig. 2.

The direct tunneling mechanism is used for the programming and erasing of the memory device with t_{tunn} = 3 nm. At room temperature and the hot temperature (85 ^oC), the device exhibits a ~1 V threshold voltage window difference under a short write / erase pulse of +12 V / -12 V for 1 μs. The device also shows good endurance up to 10^5 write / erase cycles with slight drift up in threshold voltage after 10^5 cycles. The endurance of the device is shown in Fig. 3. The threshold voltage window differences of ~1 V can also be achieved with Channel Hot Electron (CHE) mechanism for the write operation and the FN mechanism for the erase operation. During CHE programming, the gate is biased at +10 V and the drain is bias at +10 V with a programming time of 1 μs. During FN erasing, the gate is biased at -10 V for 1 μs. No drift up of threshold voltage is observed up to 10^5 cycles, as shown in Fig. 4, indicating that the device performs better under the CHE / FN write / erase mode.

The data-retention time is found to fulfill a 10-year memory window extrapolation. For the device with t_{tunn} = 7 nm, ~20 % of the stored charge will be lost after 10 years, as shown in Fig. 5; However, for the thinner tunneling oxide, i.e., t_{tunn} = 3 nm, ~70 % of the charge will be lost after 10 years, as shown in Fig. 6. For the latter case, the charge retention is not so good due to thermal tunneling of the trapped electrons through the tunnel oxide to the Si substrate.

References:
[1] S. Lombardo et. al., Microelectronic Engineering, **72** (2004) 388.
[2] R. Rao et. al., Solid State Electronics, **48** (2004) 1463.

Figures:

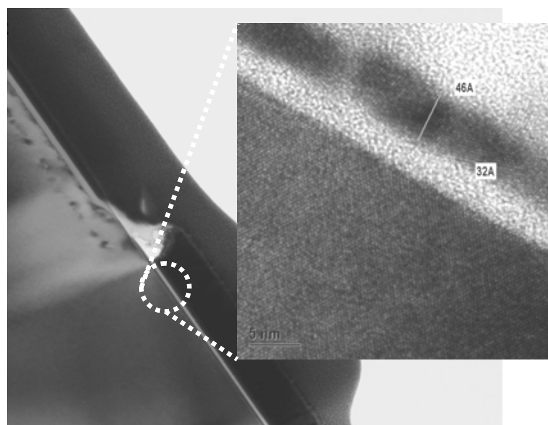

Fig. 1 HRTEM cross section of sample 2.

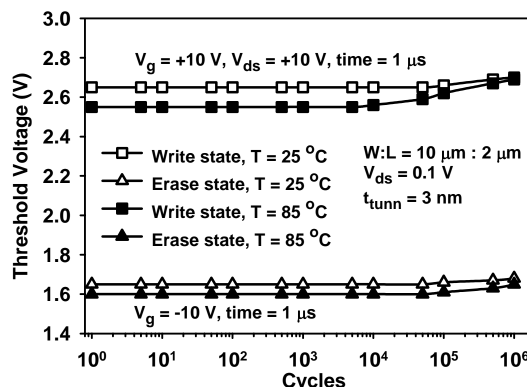

Fig. 4 Endurance performance for t_{tunn} = 3 nm. Programming / erasing operations are carried out with CHE / FN methods.

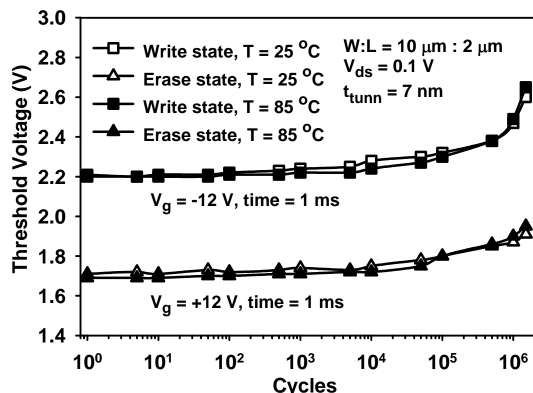

Fig. 2 Endurance performance for t_{tunn} = 7 nm. Programming / erasing operations are carried out at +12 V / -12 V for 1 ms.

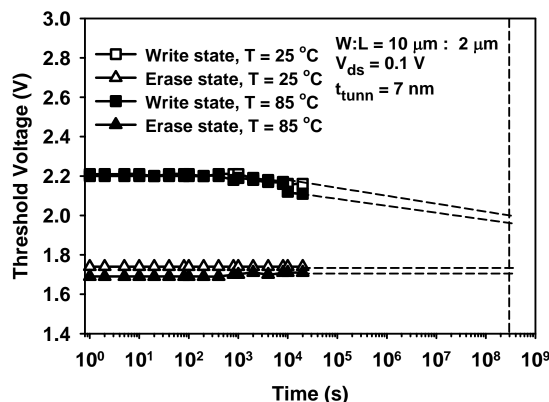

Fig. 5 Retention characteristics for t_{tunn} = 7 nm. ~20 % of charge lost after 10 years is expected.

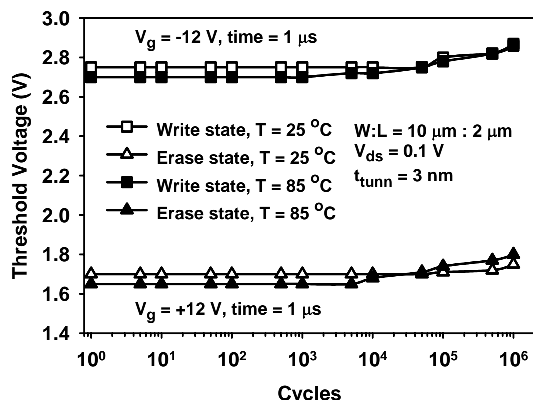

Fig. 3 Endurance performance for t_{tunn} = 3 nm. Programming / erasing operations are carried out at +12 V / -12 V for 1 μs.

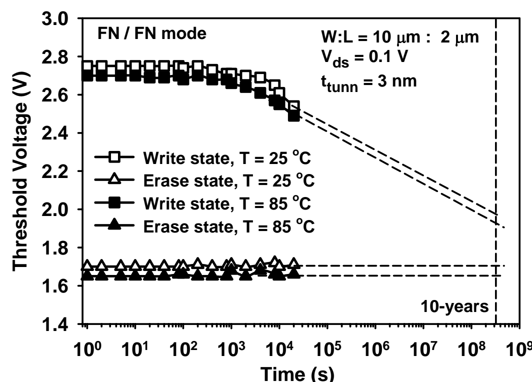

Fig. 6 Retention characteristics for t_{tunn} = 3 nm. ~70 % of charge lost after 10 years is expected.