CARBON NANOTUBE NETWORK THIN-FILM TRANSISTORS FOR HIGH-PERFORMANCE FLEXIBLE ELECTRONICS

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Single-wall carbon nanotubes (SWNTs) are unique because they are one-dimensional wires composed entirely of surface atoms yet exhibit high carrier mobilities (~10^4 - 10^5 cm^2/Vs). These extraordinary transport properties make them an ideal material for electronic applications, while their virtually infinite surface-to-volume ratio offers the possibility of extraordinary sensitivity for sensor applications. However, two main obstacles prevent their immediate commercial implementation: 1.) SWNTs as grown are a mixture of semiconducting and metallic nanotubes (depending on the helicity of the graphene sheet forming the nanotube wall), and there is no reliable technique presently available to separate them by electronic type; and 2.) it is difficult to assemble large numbers of SWNTs into precisely controlled positions. Because of these obstacles, SWNT-based devices and sensors have remained largely in the realm of impressive laboratory curiosities with limited applications.

We have developed an alternative approach to SWNT electronic and sensor applications that circumvents the problems stated above by using a random network of SWNTs as the device channel. We have demonstrated that such carbon nanotube networks (CNNs) can, by virtue of the high-quality electrical contact formed between intersecting nanotubes, form semiconducting films [1]. CNN devices circumvent the requirement of position and structural control because the devices display the aggregate properties of many randomly distributed SWNTs. An additional advantage of CNNs is the fact that they can be processed into devices of virtually any size using conventional fabrication technology, which opens a wide range of electronic and sensor applications.

Transistors fabricated from CNN films deposited from liquid suspensions on flexible polymer substrates exhibit conventional p-type FET characteristics. Typical devices (7 □m gate length, 130 □m gate width, with 100 nm SiOx gate dielectric deposited over a buried metal gate finger) have measured transconductance g_m ~ 0.5 mS/mm at V_{drain} = 1.5 V and mobility □ ~ 150 cm^2/Vs. [2] The on/off current ratio (I_{on}/I_{off}) varies from < 10 to several hundred (with occasional values >1000) for gate bias swings between -3 and +2 Volts. These relatively low values of I_{on}/I_{off} arise because the metallic nanotubes in the as-grown CNT source material create metallic (and hence ungated) conduction paths in the networks, which generate extraneous off-state currents. The wide variability in these parasitic off-state currents arises from the random distribution of the metallic nanotubes within the networks.

While large off-state currents are not critical for some uses, a much wider range of applications could be realized if these parasitic off-state currents from metallic nanotubes could be reduced, and we have investigated several techniques to achieve this. A promising approach uses weak solutions of diazonium salts to eliminate conduction selectively in metallic and small-bandgap nanotubes [3], which can lower the off-state current of CNT network transistors by several orders of magnitude while only marginally lowering the on-state current [4]. We find that several conditions are necessary for this procedure to work effectively: the CNTs should be single-walled; they should be free of hydrocarbon residue from device processing; and the CNTs should not be bundled. Our most recent efforts have

aimed at achieving these conditions with CNT networks deposited from various liquid suspensions. The implications of these promising results for the implementation of CNNs in high-performance electronics on flexible and/or arbitrary substrates, and CNN-based sensor applications [5], will be discussed.

References:

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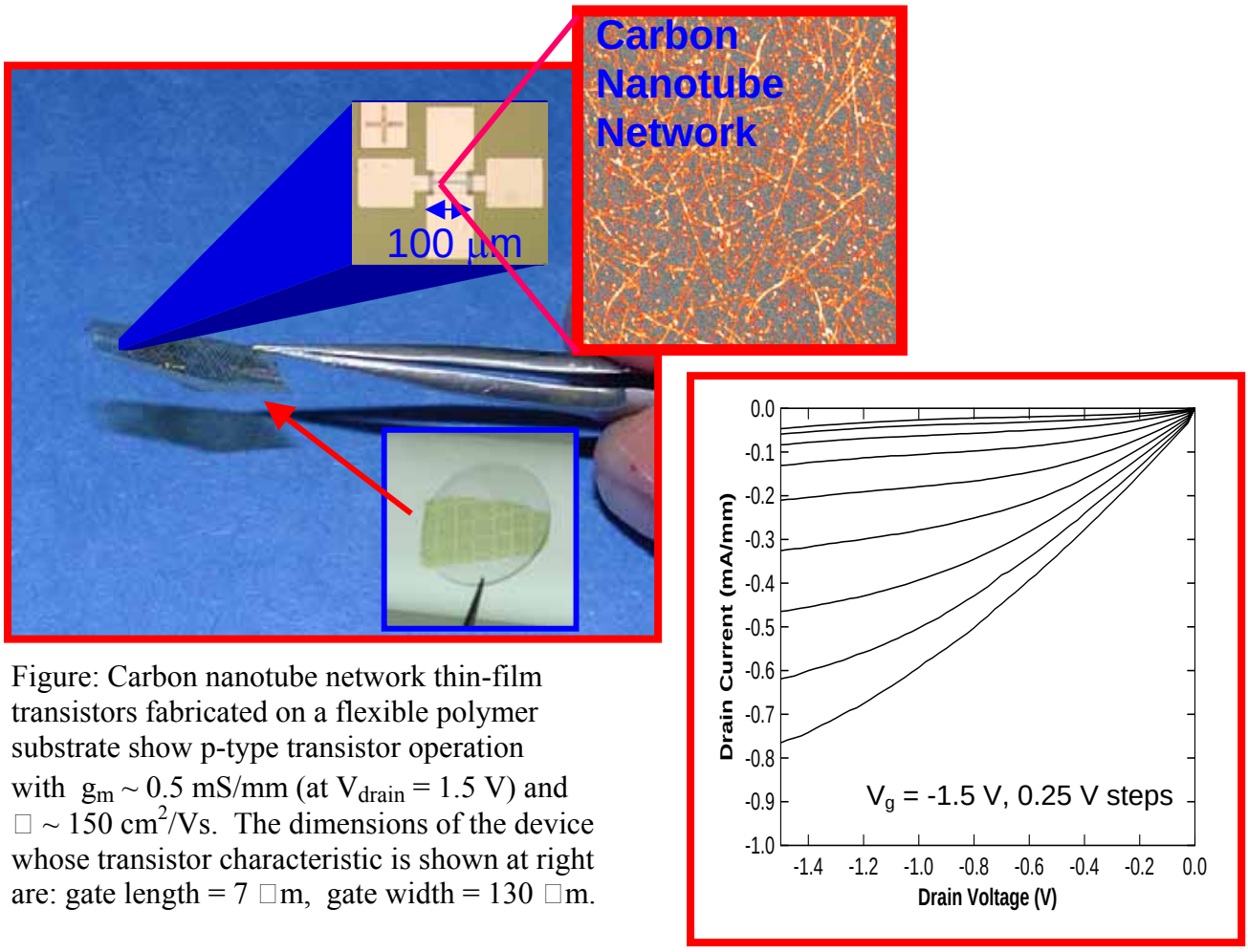

Figure: Carbon nanotube network thin-film transistors fabricated on a flexible polymer substrate show p-type transistor operation with $g_m \sim 0.5$ mS/mm (at $V_{drain} = 1.5$ V) and $\mu \sim 150$ cm^2/Vs. The dimensions of the device whose transistor characteristic is shown at right are: gate length = 7 μm, gate width = 130 μm.