Modeling of Narrow-Width SOI Devices: The Impact of Quantum Mechanical Size Quantization and Unintentional Doping on Device Operation

Dragica Vasileska and Shaikh S. Ahmed
Department of EE, Arizona State University, Tempe, AZ 85287-5706, USA
E-mail: vasileska@asu.edu, Shaikh.Ahmed@asu.edu

The ultimate limits in scaling of conventional MOSFET devices have led the researchers to look for novel device concepts such as dual-gate SOI devices, FinFETs, focused ion beam MOSFETs, etc. These novel devices suppress some of the short channel effects exhibited by conventional MOSFETs. However, a lot of the old issues remain and new issues begin to appear. For example, in both dual-gate SOI MOSFETs and in FinFET devices, quantum mechanical size-quantization effects significantly affect the overall device behavior. In addition, unintentional doping leads to considerable fluctuation in the device parameters, and the electron-electron interactions affect the thermalization of the carriers at the drain end of the device. In this work, we have investigated the influence of these relatively new and challenging issues on the operation of a narrow-width SOI device structure from Fig. 1 [1].

When simulating this device, to take into account the quantum-mechanical size-quantization effects along the depth and the width of the device, we have utilized the *effective potential* approach due to Ferry [2] that has been incorporated into our existing 3D Monte Carlo particle-based simulator and tested on a variety of devices. The incorporation of the effective potential gives rise to two effects: reduction of the electron density and a set back of the charge from the interface. The presence of a two-dimensional carrier confinement results not only in a significant increase in the threshold voltage (~180 mV for a device with 10 nm channel width, as depicted in Fig. 2 – top panel), but also in its pronounced channel width dependency (Fig. 2 – bottom panel) that is observed experimentally and confirmed with our simulations.

Another issue that poses serious problems in conventional MOSFETs is that the dopant distribution in ultra-small devices can no longer be regarded as statistically uniform. Variations in the doping arrangement will make it harder to predict the device performance and will create transistor mismatches. The solution to this problem in SOI device structures is to use undoped silicon films. However, as shown in this study, an unintentional doping, i.e. the presence of even a single impurity atom can alter the performance of the device under consideration. The impurity position dependence of the drain current is shown in Fig. 3. There are several noteworthy conclusions that can be drawn from these simulations: (a) Due to the size-quantization effect, which results in the majority of current flowing through the center portion of the channel, a dopant ion trapped in the center of the channel produces maximum fluctuations, (b) Single impurity at the source end of the channel affects the drain current most and produces maximum shift in the threshold voltage, and (c) The largest effect is in the subthreshold/weak-inversion regime, where the density of the mobile carriers is very low. As the drain current increases, the electrons in the channel begin to screen the localized potential of the single dopant ion reducing its impact on the current flow. The width dependence of the device threshold voltage, for the case of a discrete impurity distribution, is shown in Fig. 4. These results suggest that both quantization effects and discrete impurity effects must be included in the theoretical model to properly describe the experimental threshold voltage data.

Regarding the electron-electron and electron-ion interactions, we find that they affect the carrier energy/velocity near the drain end of the channel (Fig. 5). Note that in our 3D Monte Carlo particle-based device simulator, we have implemented two schemes that properly account for the short-range electron-ion and electron-electron interactions: the corrected-Coulomb approach and the P^3M method [3,4].

References:

[1] H. Majima, H. Ishikuro and T. Hiramoto, IEEE Electron Dev. Lett., **21** (2000) 396.
[2] D. K. Ferry, R. Akis and D. Vasileska, IEDM Tech. Dig. (2000).
[3] W. J. Gross, D. Vasileska and D. K. Ferry, IEEE Trans. Electron Dev., **47** (2000) 1831.
[4] R. W. Hockney and J. W. Eastwood, Computer Simulation Using Particles, New York, McGraw-Hill, 1981.

Figures:

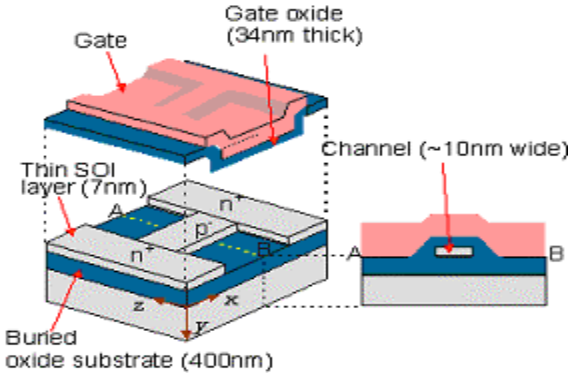

Figure 1. Schematic description of the device structure being simulated in this study. The thickness of the silicon on insulator layer is 7 nm, with p^- region width ranging between 5 and 20 nm. The channel length is 50 nm and the doping of the p^- layer equals 10^{16} cm^{-3}.

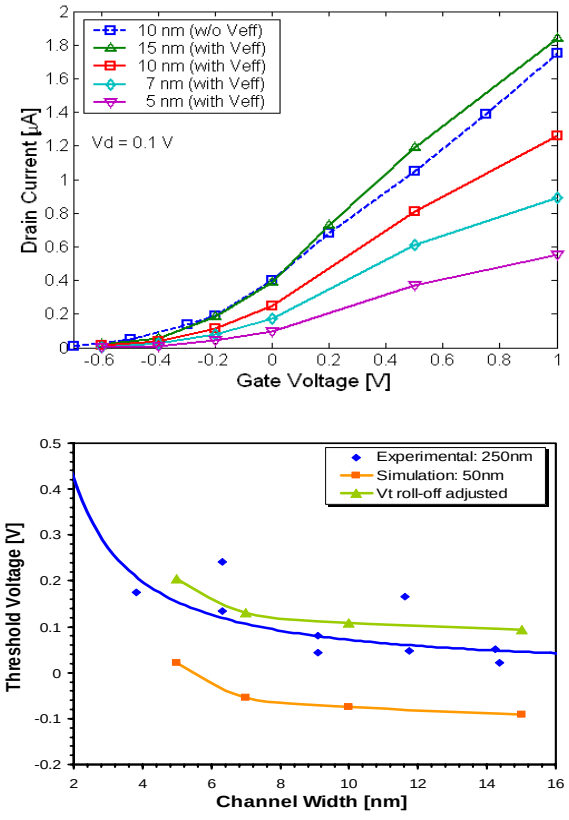

Figure 2. (top panel) Transfer characteristics of devices with 5, 7, 10 and 15 nm channel width. (bottom panel) Variation of the threshold voltage with channel width.

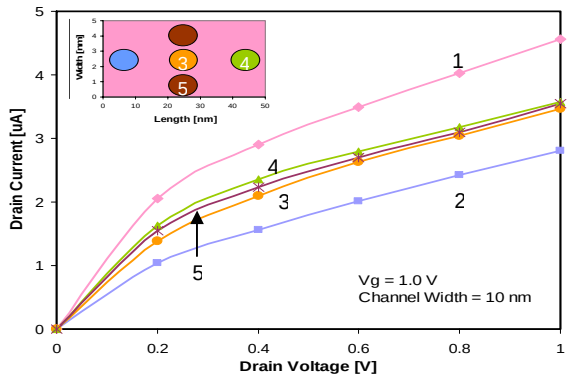

Figure 3. Device output characteristics using continuum and discrete impurity model.

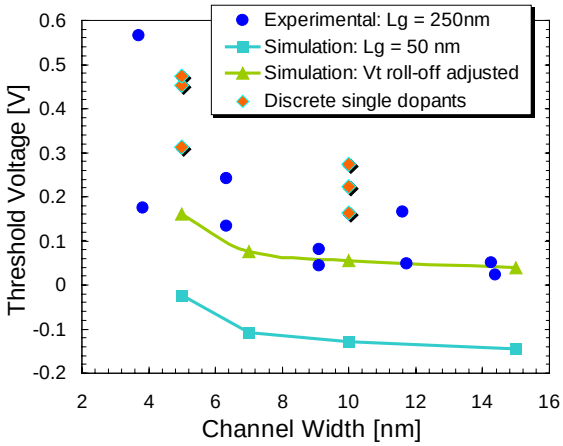

Figure 4. Width dependence of the threshold voltage for the case of uniform and discrete impurity model.

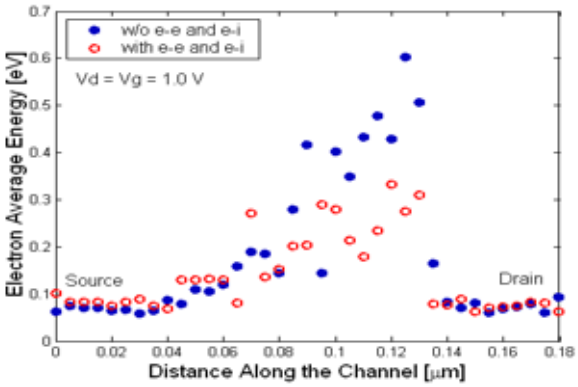

Figure 5. Electron average energy along the channel showing the influence of e-e and e-ion interactions (channel length = 100 nm).