

**CONDUCTANCE QUANTIZATION IN Si/SiGe BENDED WIRES**

E. Giovine<sup>1</sup>, R. Leoni<sup>1</sup>, G. Scappucci<sup>2</sup>, L. Di Gaspare<sup>2</sup>, A. Notargiacomo<sup>2</sup>, F. Evangelisti<sup>1,2</sup>,  
<sup>1</sup>Istituto di Fotonica e Nanotecnologie, IFN-CNR, V. Cineto Romano 42, 00156 Roma, Italy  
<sup>2</sup>Unità INFM, Dipartimento di Fisica "E. Amaldi", Università Roma TRE, V. Vasca Navale  
84, 00146 Roma, Italy

Fabrication and characterization of single electron transistors (SET) has been an area of considerable interest in recent years. A variety of configurations have been proposed in order to realize well performing devices. We have shown recently that a "bended wire" geometry gives rise to "robust" tunneling barriers inside the wire itself and can be employed for the realization of SET's based on Si/SiGe heterostructures [1].

In the experimental quest of the most favorable configuration resulting in suitable barriers for SET behavior we have fabricated a series of "bended" wires and have investigated their electrical transport. The adopted geometry is shown in Fig.1. Starting from modulation-doped Si/SiGe heterostructures containing a high-mobility two-dimensional electron gas the devices were fabricated by electron-beam lithography and dry etching. Two bends are introduced by displacing laterally the central segment of the wire. In the device of Fig. 1 the 550-nm-long central region of a 250-nm-wide wire is displaced by 180 nm. The shift results in two constrictions with a geometrical width of 70 nm, connecting the central region with the other two segments of the wire and the outer mesa structure. Due to sidewall depletion caused by the fabrication process, the constrictions have an effective width smaller than the lithographic one so that, concerning electronic transport, they act as quantum points contacts (QPC) or tunnelling barriers, depending on their potential. In order to vary the central region potential, the devices were completed by depositing a 25-nm-thick SiO<sub>2</sub> layer on the sample and a central aluminum control gate aligned with the cavity. The devices were shaped so as to allow electrical characterization both in a two and four terminal configuration.

In Fig.2 we report the two-terminal conductance as a function of the gate voltage at T=50mK, exhibiting a non-integer conductance staircase, whose step height decreases upon increasing the gate bias. These features indicate that the constrictions act as quantum point contacts connecting the cavity to the source and drain. The measurements can thus be explained interpreting the staircase dependence as a fingerprint of conduction quantization due to the two QPC's and ballistic transport. Due to the large dimensions of the central region no evidence of Coulomb blockade effects were found in the first series of devices investigated. Devices of smaller size are being investigated presently.

**References:**

- [1] A. Notargiacomo, L. Di Gaspare, G. Scappucci, G. Mariottini, F. Evangelisti, E. Giovine and R. Leoni, *Appl. Phys. Lett.*, **83** 302 (2003).

## Figures:

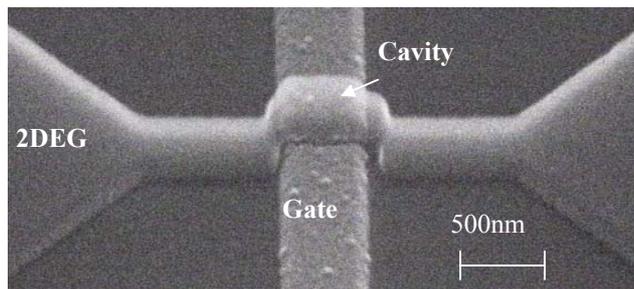


Fig. 1. Scanning electron micrograph of a cavity fabricated by reactive ion etching of a Si/SiGe modulation doped heterostructure.

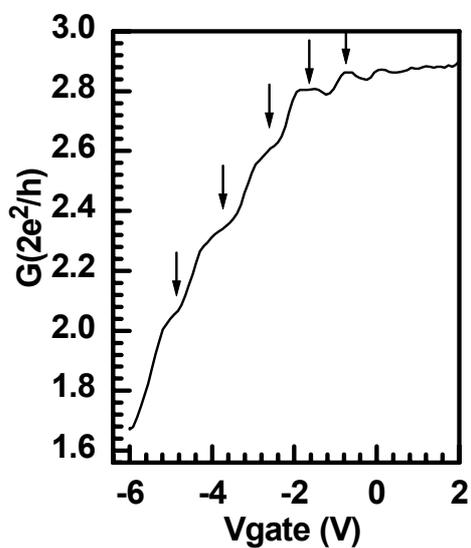


Fig. 2. Two-terminal conductance vs. gate voltage  $V_{gate}$  measured at 50 mK. The step-like dependence is interpreted in terms of quantization of the conductance due to the two QPC's connected in series by the cavity.