

ELECTRON BEAM LITHOGRAPHY FOR APPLICATIONS IN NANOTECHNOLOGY

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Nanotechnology, apart from being a catch phrase for media and funding, has a serious role for the development of future products in the field of information technology. Specifically, future generations of memory and logic chips depend strongly on the ability of nanolithography. In addition to the promising field of nanoelectronics, optoelectronics as well as photonic devices benefit from the potentials developed in nanoscaled processing. A central role in this field plays electron beam lithography (EBL) as a pioneering nanolithography tool as well as the lithography with the highest resolution up to now.

The talk starts with a report on the current state of EBL performed with an optimally tuned Leica EBPG-5000 TFE electron beam system [1]. The fabrication of structures with critical dimension below 10 nm in high resolution negative tone electron beam resist Hydrogen silsesquioxane (HSQ) is described. Later on line edge roughness, overlay accuracy and process conditions necessary to achieve this high resolution lithography are reported.

A full process sequence for the fabrication of functional nanostructures is addressed in the next part. Specifically, a new method of resist drying is addressed. Improvements by megasonic-assisted development with respect to homogeneity, depth and quality of nanostructures are presented.

As the success of nanoelectronic will depend critically on the availability of low cost manufacturing tools, next generation lithography tools based on nanoimprint have strategical importance. There the EBL acts as primary lithography step for the mold fabrication. A nearly one to one correspondence between the mold and the transferred silicon pattern can be achieved down to about 10 nm. The process suitability of the UV-NIL technique is demonstrated by the fabrication of functional Triple-Gate n-MOS transistors with channel widths down to 50 nm [2].

The best way to test the quality of nanolithography processes is to study the function of certain electronic components. Therefore, pattern transfer, most critical during the realization of nanoelectronic components, is checked routinely by creating functional test patterns that allow direct access via electrical characterization. In the talk two examples are presented.

In the field of nanoelectronics this is the Electrically variable shallow Junction MOSFET (EJ-MOSFET). EJ-MOSFETs are attractive test devices to investigate the scalability of MOSFETs down to the deca-nanometer regime. Here sophisticated techniques for the implantation and activation of source and drain regions are

avoided with a second gate electrode on both sides of the conventional transistor gate, which electrically activates ultra shallow junctions. EJ-MOSFETs on Silicon-On-Insulator (SOI) material with a gate length of 12 nm are shown [3]. The transition from a quasi planar MOSFET to a Triple-Gate design is experimentally investigated by narrowing the active channel to a width of 30nm. Triple-Gate EJ-MOSFETs with undoped channels display decisively suppressed short channel behavior at 12 nm gate length compared to their planar counterparts (Fig 1). The devices fabricated exhibit extremely low off currents and 8 orders of magnitude between the on and off state. This demonstrates the potential for MOSFET structures in the 10 nm regime.

Finally, as an example in the field of nanophotonics the fabrication of ultra low loss SOI microring resonators via EBL and HSQ with extremely high Q factor is described (Fig. 2). [4].

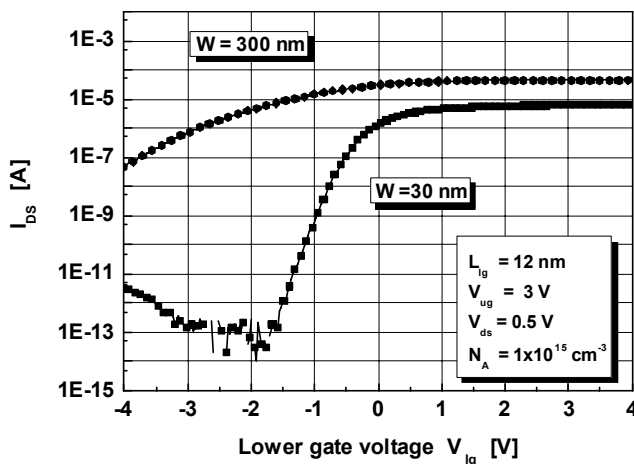


Figure 1: Comparison of the transfer characteristics of a planar EJ-MOSFETs and a Triple-Gate EJ-MOSFET at low channel doping.

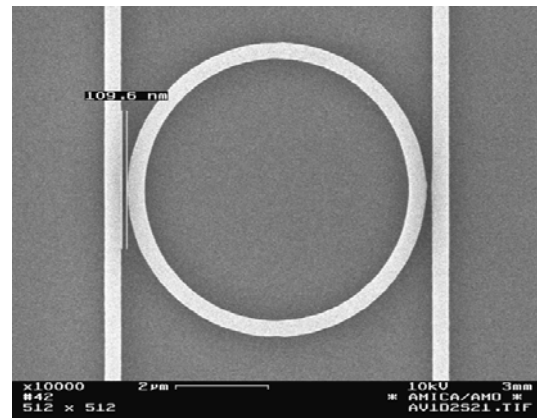


Figure 2: Scanning electron micrograph of an SOI microring resonator

References

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