Fabrication and Application of Silicon Single-Electron Devices

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Fabricating silicon single-electron transistors (SETs) by using MOS processes is advantageous because we can use highly advanced fabrication tools developed for CMOS LSIs [1]. We have developed a MOSLSI-compatible fabrication process for SETs based on pattern-dependent oxidation (PADOX) [2, 3]. Figure 1 shows the SET structure and the formation mechanisms. We exploit quantum size effect in a narrow Si wire and the band-gap reduction afforded by the huge stress accumulated during the oxidation. Figure 2 shows the drain current oscillation characteristics of a Si SET measured as a function of gate voltage V_{gs}.

The special feature of Si SETs is that these electrical characteristics are very stable due to the absence of offset charges [4]. It has been believed that the greatest drawback of SETs is offset charge instability. However, as shown in Fig. 3, we have obtained a monotonic relationship between the first-electron-peak voltage V_{fp} and gate capacitance C_g measured for several SETs whose C_g shows an almost linear relation to the island size [5]. This implies that threshold voltages of SETs are controlled by SET sizes, which is indispensable in practical application of SETs.

This fabrication process for SETs based on PADOX allows us to combine SETs with conventional MOSFETs, which will be useful in the practical application of SETs as an interface with the real world. We have employed MOSFETs in combination with SETs to emphasize the special functionality of SETs [1]. We have demonstrated multiple-valued logic circuits by combining a SET with a small MOSFET.

Multiple-valued operation allows us to reduce the number of transistors and the amount of wiring in LSIs. To achieve it, we need devices that have multiple stable points. The oscillatory characteristics of a SET are applicable for this purpose. Figure 4 shows a basic element for a multiple-valued circuit and its two-terminal *I-V* characteristics [6]. It is advantageous that, within the breakdown voltage, the number of stable points is infinite in principle. By using the element, some logic applications, such as single-electron quantizer and an A-D converter, have already been demonstrated [6].

In summary, we have demonstrated some of the advantages of Si SETs, such as relatively high temperature and stable operation, and high functionalities. The combination of SETs with MOSFETs is useful in expanding applications of SETs. We have also achieved single-electron transfer devices consisting of small MOSFETs and SETs [7-10]. These devices will enable us to make future LSIs with highly functionality and low power consumption nature.

References:

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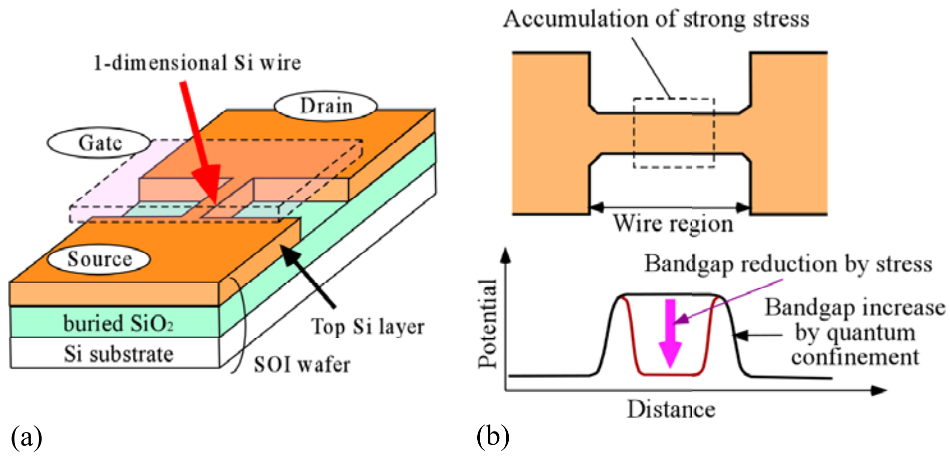

Fig. 1. Initial device structure of the SET before oxidation (a), and schematic plane view of the device and potential diagram along the Si wire (b). A Si wire is converted to a small SET by quantum size effect and band-gap reduction due to the huge stress accumulated in the wire during the thermal oxidation.

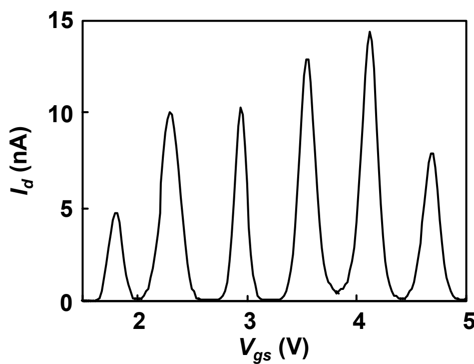

Fig. 2. Drain current I_d as a function of gate voltage V_{gs} of a Si SET fabricated by the PADOX process measured at drain-source voltage V_{ds} of 5 mV at 27 K.

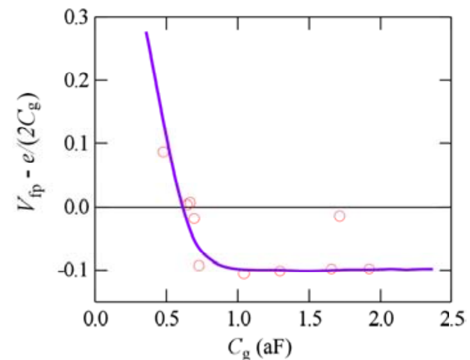

Fig. 3. Relation between gate voltage for the first electron peak V_{fp} and gate capacitance C_g. V_{fp}-$e/2C_g$ corresponds to the threshold voltage when the charging effect is subtracted.

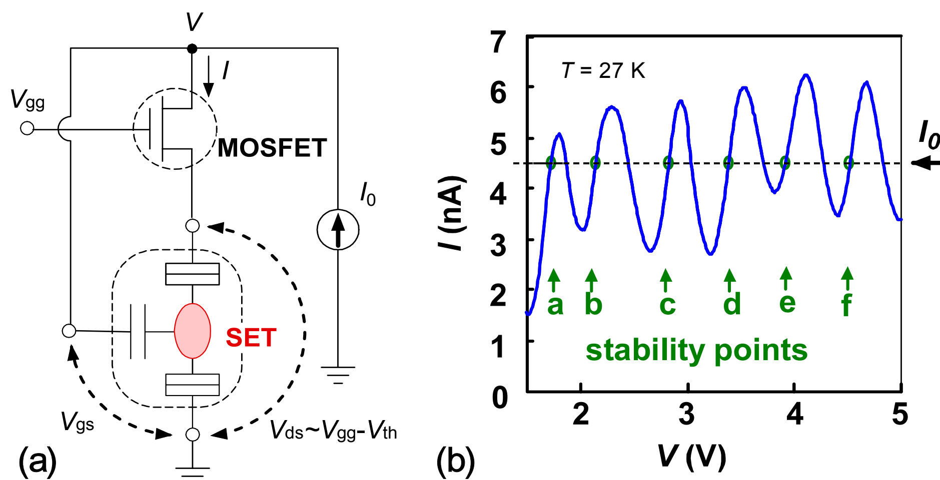

Fig. 4. Basic element of multiple-valued memory and its current-voltage characteristics measured at 27 K. We combine a SET with a MOSFET to keep the drain voltage of the SET low enough to sustain a Coulomb blockade. When the constant current source I_0 is connected, points **a-f** are stable.