

SEMICONDUCTOR NANOCRYSTALS IN ULTRA THIN SiO₂ LAYERS FOR NON-VOLATIVE MEMORY APPLICATIONS

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In order to respond to the increased requirements in applications of non-volatile memories and to overcome the limitations of current technology, different devices and technologies are under investigation. Among the alternatives intensively investigated is the use of two-dimensional arrays of silicon nanocrystals embedded in thin SiO₂ layers as a distributed charge storage medium to replace the polycrystalline silicon floating gate in a conventional memory cell. Semiconductor nanocrystal memories offer important advantages related to the possibility to use thinner tunneling oxides, due to the electrical discontinuity of the charge storage medium. These are: a) faster write-erase times, b) smaller degradation, c) better compatibility with ULSI scaling and d) lower operating voltages and lower power consumption. Different processing techniques are explored during the last few years for the fabrication of two-dimensional arrays of embedded semiconductor nanocrystals of a given size and density in SiO₂, with a controlled thickness of the two barrier oxides. Among these techniques the most promising seem to be a) ion beam synthesis (IBS) in the ultra-low-energy (ULE) regime [1,2] and b) low pressure chemical vapor deposition (LPCVD) of silicon on SiO₂ [3-7]. In this last case, quantum dots are either directly grown on SiO₂ [3-5] or an amorphous layer is deposited, followed by high temperature oxidation and crystallization [6-7]. Differences are observed in the material fabricated in each case, which strongly affect the charging and retention properties of the memory cells. Full understanding of the mechanisms involved in charge storage is necessary in order to control device properties. In this respect, model structures composed of ordered 2-D arrays of Si or Ge quantum dots embedded in SiO₂ are under investigation within the IST FORUM FIB project and results will be discussed.

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