ELECTRICAL CHARACTERISTICS OF SILICON NANOWIRES FABRICATED ON THINNED SOI SAMPLES BY AFM LITHOGRAPHY

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Silicon nanowires can be fabricated on an insulating surface by AFM lithography. This technique is a two-step process. The first step consists in the generation of an oxide mask on a H-passivated silicon sample by AFM induced local anodisation under the biased conductive tip [1-3]. Then, this mask can be transferred to the silicon sample by a step of silicon wet etching in a TMAH solution, selectively regarding silicon oxide. Starting from SOI sample, this technique allows to pattern insulated silicon nanowires [4-5]. An advantage of SOI sample is the possibility to use the back silicon bulk as an extra gate called 'backgate'. The resolution reached by this lithography technique can be as high as 10 nm [6].

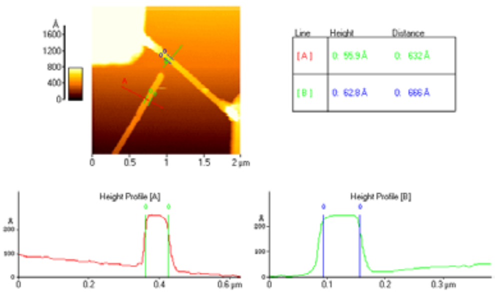

Figure 1 : Lateral gate Field Effect Transistor fabricated by AFM lithography.

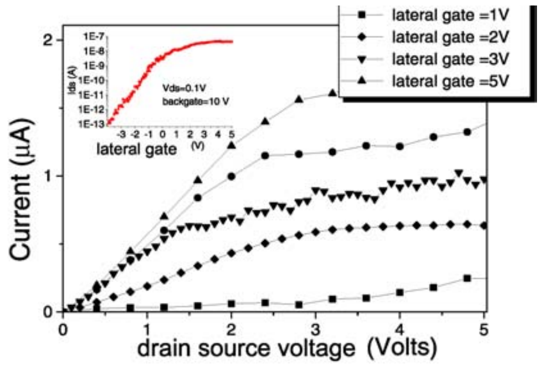

Figure 2 : Electrical characteristics a lateral gate FET whose channel doping level is 2.10^{17} cm^{-3}.

We have used this technique to draw connected silicon nanowires (figure 1) to carry out electrical characteristics of the wires at room and low temperature (4 K). Two different doping levels have been studied : 2.10^{17} and 10^{19} cm^{-3}. At room temperature the device shown in figure 1 has the behaviour of a Field Effect Transistor with a lateral gate (figure 2). The light influence on wire conductivity has also been studied (figure 3). It was observed that, although the thin wires are in crystalline silicon (as demonstrated by TEM analyses), the behaviour of the wires under illumination is similar as in the case of a:Si-H : the dark current of the wires decrease after illumination (similar to Staebler-Wronski effect).

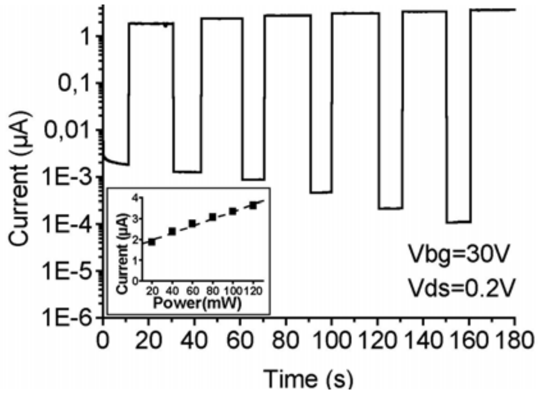

Figure 3 : Drain-source current variations with time operating alternatively under illmunation or in dark conditions. The light intensity varied from 20 to 120 mW by step of 20 mW. The drain source bias was fixed at 0.2 V.

At low temperatures, a gap is open in I-V curves at low voltage (figure 4). The value of the gap is thermally activated and the phenomenon is attributed to Coulomb blockade effect in the structure. In fact, at lower temperatures (4K) and under a constant bias voltages V_{DS} lower than 5mV, conduction peaks (see Fig.4, inset) separated by a perfectly insulating behavior are observed in I-$V_{backgate}$ curves. The aperiodicity of the oscillations are attributed to the random distribution of dopants along the wire which is responsible for large potential fluctuations along the wire and leads to potential wells centered around dopants.

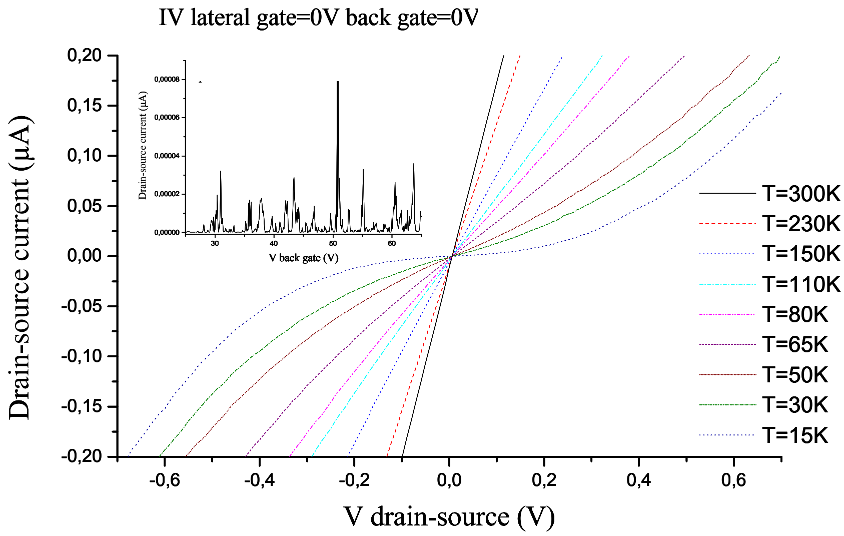

Figure 4 : Low temperature I_{DS}-V_{DS} characteristics. Inset I_{DS} oscillations when the backgate voltage is swept.

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