

ELECTRON BEAM DIRECT WRITE LITHOGRAPHY FOR SEMICONDUCTOR MANUFACTURING : SOLUTION TO ANTICIPATE ARCHITECTURE DEVELOPMENT FOR 32nm NODE AND BELOW

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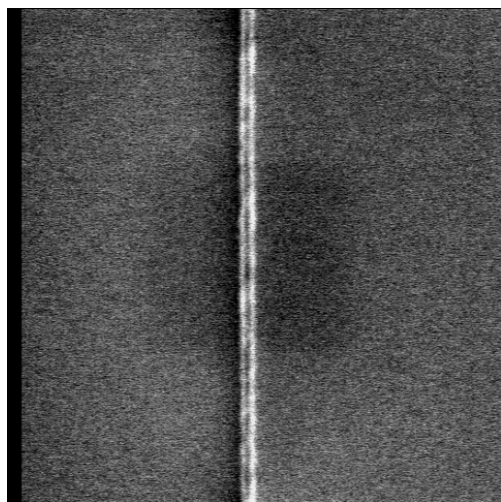
The speed up of the International Table Roadmap for Semiconductor (ITRS) for the introduction of new generation node maintains a strong pressure on lithography manufacturers to provide on time industrial solutions able to answer to the even more aggressive specification targets. Optical lithography is expected to be the dominant approach potentially down to the 32nm node with the introduction of the immersion tools. However, mask complexity and price escalation due to mask error increase and strong reticle enhancement techniques implementation, seriously impact lithography budget that could reach more than 50% of overall manufacturing costs for the 32nm node(1).

In this context, direct write lithography can be applied for specific applications to reduce cost pressure in architecture development and non recurrent applications, like low volume ASIC, customization... Gaussian electron beam systems are today widely used in R&D laboratories for R&D activities. Two Gaussian systems, working with an accelerating voltage of 50 and 100kV, are today operational in the CEA-LETI facilities, allowing answering to various types of programs. A review of the lithography cell capability (Fig.1) will be presented showing that the high resolution capability of the Gaussian beam systems linked with optical lithography solution represent one alternative to answer to aggressive R&D applications.

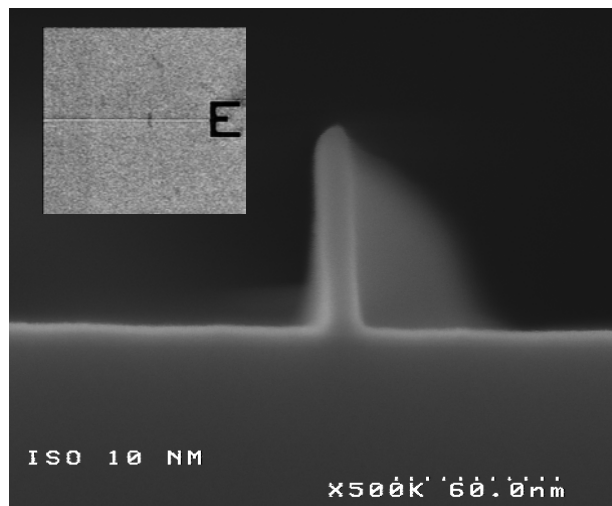
However, the main drawback of Gaussian systems is the very low throughput capability that definitively cannot match the cycle time constraints of standard ASIC production environment. The insertion of shape projection principle, already widely used for mask manufacturing, represents one alternative for direct write lithography to deliver high resolution associated with reasonable throughput capability. A first shape beam system was installed current 2001 at Crolles site to answer to the common programs between Philips Semiconductor, Freescale Semiconductor and STMICROELECTRONICS. Important validation work (2) was performed to demonstrate the maturity of this technology and its compatibility with difficult production environment (Fig. 2). Finally, low cost process flow based on a co-integration of E-Beam and Optical lithography are now qualified and able to answer to a large field of application, as, for example, the support for the preliminary development phases of a new generation node. An overview of this integration activity will be presented showing that EBDW activity can play a role for low cost ASIC manufacturing as well as advanced R&D activity.

(1) S. Hector; 7th IFST symposium;

(2) L. Pain et al, Proc. SPIE, paper 5374-63, to be published (2004)

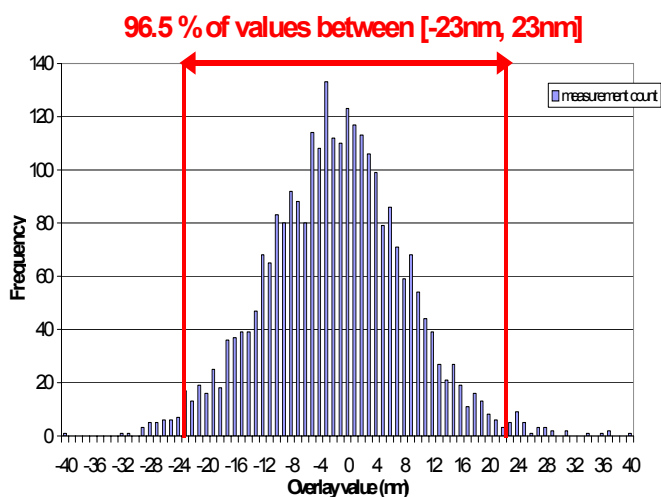


Standard chemically Amplified resist
CD 20 nm

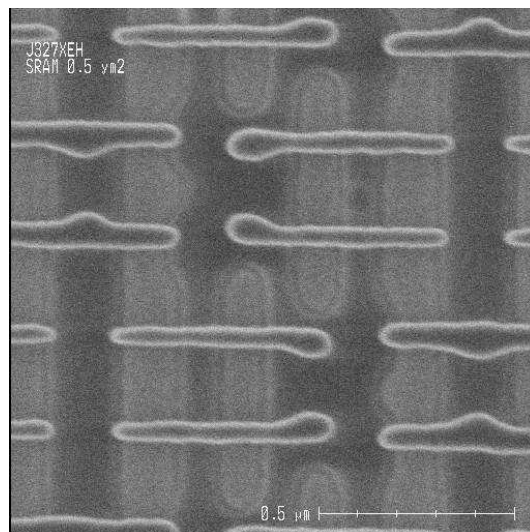


HSQ type resist
CD : 10 nm

Figure 1 : Gaussian Beam ultra high resolution capability overview



Gate on active overlay capability presentation
On 65nm production lot
ITRS overlay target : [-23nm, 23nm]



Gate on Active EBDW patterning
overview after etch step on 65nm SRAM
cell
Gate size 45nm

Figure 2 : Shape Beam integration capability overview