SINANO: SILICON-BASED NANODEVICES EUROPEAN NETWORK OF EXCELLENCE OF THE 6TH FRAMEWORK PROGRAMME

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The European Network of Excellence of the 6th Framework Programme (SINANO – Silicon-based Nanodevices) aims to strengthen scientific and technological excellence in the field of electronic, Si-based nanodevices for terascale integrated circuits (ICs). SINANO started on January 2004 with 41 partners from 16 European countries [1].

There are very difficult challenges in pushing the limits of silicon integration down to nanometric dimensions over the next quarter century (see for instance the European Technology Roadmap for Nanoelectronics and the International Technology Roadmap for Semiconductors [2,3]). These are addressed by integration at the European level of the research capabilities, technology and characterisation platforms principally existing in the main university and research centres in this field.

The activities of this Network are oriented towards long-term and multidisciplinary objectives relevant to realising nanoelectronics on Si-based substrates. Such work involves new silicon platforms (i.e. Silicon-On-Insulator (SOI), relaxed Silicon-Germanium (SiGe) "Virtual Substrates" (VS)) and alternative channel materials (e.g. strained Silicon, SiGe, SiGeC).

This activity could herald a revolution in future ICs - integrating Si-based classical and innovative ultimate CMOS devices, and the emerging post-CMOS memory and logic nanodevices. This ambitious research programme can only be achieved by using a Network with a critical mass for such work, and will underpin the technology and the economy for the foreseeable future.

The research carried out in the network typically deals with structures in the range of 1-40 nm and is concerned with all the relevant topics for device optimisation: nanotechnology, physics of nanodevices, modelling and simulation, nano-characterisation and new materials for Si-based device integration. The best European teams are working together on these multidisciplinary topics with a view to enhancing device integration, functionality and performance needed to meet future demands of communication and computing.

The research are performed on devices and structures relevant to Si-based ultimate-CMOS and complementary non-CMOS fields. There are many interactions and common themes in these areas, and it is very valuable and opportunistic to join up and coordinate efforts to gain the understanding that enable optimisation of the following nanodevices and nanostructures:

- New channel materials for ultimate CMOS (SiGe, strained Si, Si:C and SiGe:C)

- Non-classical nano-MOSFET architectures (SOI (Silicon-On-Insulator), SON (Silicon-On-Nothing), double-gate, gate-all-around, FinFET, vertical structures)

- Emerging post-CMOS logic and memory nanodevices (*Single electron devices* : SET (Single Electron Transistors), SET & CMOS hybrids, SEM (Single Electron Memory), Nano-floating gate memory, QCA (Quantum Cellular Automata)-cells; *Quantum devices* : RTD (Resonant Tunnelling Devices), Ballistic junction devices, Spin-polarization devices).

In the nano-CMOS area, the activities of the network focus on ultimate MOSFETs in the sub-40 nm gate length range for very high frequency and low power applications. Traditional bulk Si MOSFETs pushed towards their limit are studied. In this respect, the analysis and optimization of high-k gate dielectrics are needed for the integration of these devices. Metal gates are also a possible solution to overcome the limitation of polysilicon.

However, other approaches are studied for the ultimate integration of silicon. The SOI-like structures are very good candidates for decananometer MOSFETs. In this respect, ultra-thin SOI MOS transistors and volume-inversion based devices (double gate, gate-all-around, FinFET) would seem to be the best devices in order to reduce short channel effects and improve current drive, and are realized and investigated in the sub-40 nm regime. Other novel materials and architectures such as strained Si, SiGe, SON and vertical devices are also studied for breaching the limits of device integration.

Emerging Si-based logic and memory devices, which could be used together with CMOS on the same chip or as post-CMOS solutions for improving integration and/or performance, are also investigated. These nanostructures are realized by modified top-down or new bottom-up approaches. In particular, single electron devices are the ultimate electron devices and are fabricated with nanometric dimension for room temperature operation. Quantum devices (Si-based resonant tunneling, ballistic junction and spin polarisation devices) are also realized and studied.

To improve our knowledge, the physical mechanisms which are observed and can govern the transport properties and the performance of both ultimate CMOS and post-CMOS, such as Coulomb blockade and resonant tunneling, are investigated simultaneously in these nanodevices. The study of alternative memory devices will also help to overcome the limitation of present memories. Si-based nano-floating gate structures and single electron memories are thus realized and analyzed in SINANO.

References :

1. See the web site : www.sinano.org
2. International Technology Roadmap for Semiconductors, 2003
3. Technology Roadmap for Nanoelectronics, 2001