ELECTRON BEAM LITHOGRAPHY FOR THE FABRICATION OF NANO-SCALE FINFET DEVICE DEMONSTRATORS

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Multi-gate transistors are considered to be the ultimate device concept for use in future CMOS generations. The so-called FinFET [1] is a variant with a straightforward process flow [2]. A three-dimensional sketch of the FinFET can be seen in Fig.1. The small channels benefit from superior electrostatic channel control, resulting in enhanced turn-off behavior. However, its fabrication demands excellent lithography and etching techniques, since very small fins with smooth vertical sidewall surfaces, that define the channel region, have to be fabricated. Furthermore for the fabrication of a minimal device the overlay accuracy must be in the range of the fin width.

Electron beam lithography marks and optical alignment marks for all subsequent lithography steps are predefined with optical lithography on an SOI wafer with 50nm top silicon and etched into 100nm buried oxide. This topographic step yields sufficient secondary electron contrast of the alignment marks for an SEM based electron beam lithography at 10 keV with 100 nm thick calixarene resist [3]. The fin is exposed with electron doses around $2 mC/cm^2$, pattern transfer is performed with high density plasma reactive ion etching into the hard mask stack of 20 nm Si_3N_4 (only for the double gate) and 40 nm SiO_2 and – after resist removal – into the mono-crystalline top silicon layer [4]. After removal of the etching passivation layer and thermal oxidation with 3 nm gate oxide, in-situ doped poly silicon is deposited with either phosphorous doping for the pMOS or boron doping for the nMOS transistor. A second e-beam lithographic step comparable to the one described above is accomplished with 10 nm overlay accuracy by in-situ scan-field correction on the 80 nm hard mask and 150 nm calixarene resist [5]. The gate is etched using a process similar to the fin etch and the source and drain regions are implanted ($3\cdot10^{15} cm^{-2}$ arsenic for n-channel, boron for p-channel, followed by a 1000°C anneal) prior to back-end processing. An SEM image of a test transistor is shown in figure 2. TEM cross-sections of a finished device (after back end processes) can be seen in figure 3 and figure 4.

Figure 5 shows the output characteristics of typical FinFET devices with 25 nm (nMOS) and 20 nm (pMOS) fin width and gate lengths of 20 nm (nMOS) and 30 nm (pMOS). The width of the device is calculated using twice the fin height plus the fin width for current normalization. Maximum on-currents of 1.6mA/µm (nMOS) and 0.6 mA/µm (pMOS) can be achieved. The sub-threshold slopes reach typically values of 80 to 100 mV/dec. Low off-currents down to 3 pA/µm (nMOS) and 0.4 pA/µm (pMOS) have been achieved. The threshold voltages V_t amount to 1.4 V for nMOS and 0.9 V for pMOS.

The first FinFETs with an excellent overlay accuracy of 10 nm allowing minimum transistor areas have been fabricated. By varying the application flow slightly either double-gate FinFETs or tri-gate FinFETs can be fabricated. The output characteristics show excellent on-currents. Hence, the FinFET is perfectly suited for CMOS applications at 45 nm and below.

References

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[5] J. Kretz, L. Dreeskornfeld, J. Hartwich, W. Rösner. Microel. Eng. 67-68, p.763 (2003).

Figures

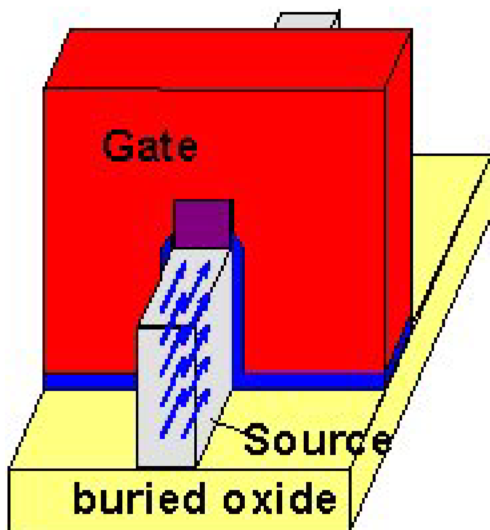

Figure 1: Schematic of FinFET.

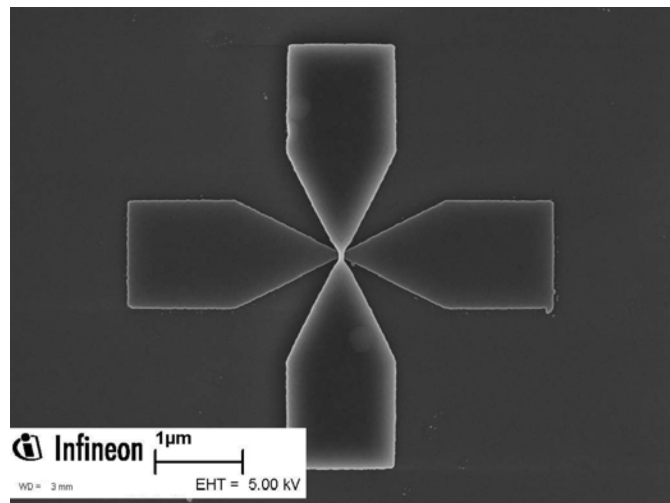

Figure 2: SEM of a FinFET test structure with connecting pads.

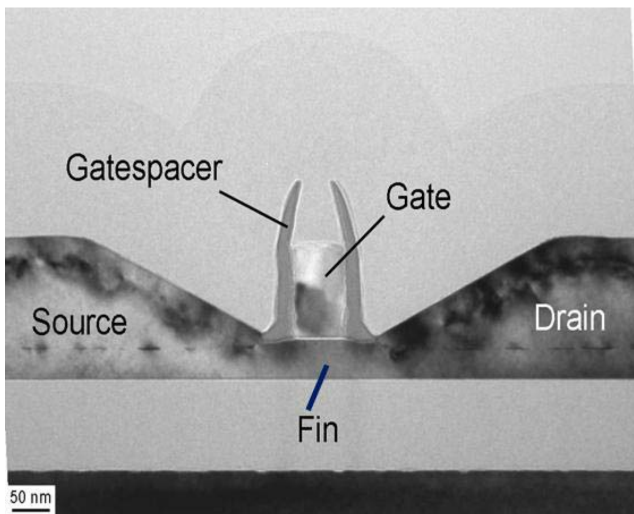

Figure 3: TEM cross section of a FinFET through source-drain.

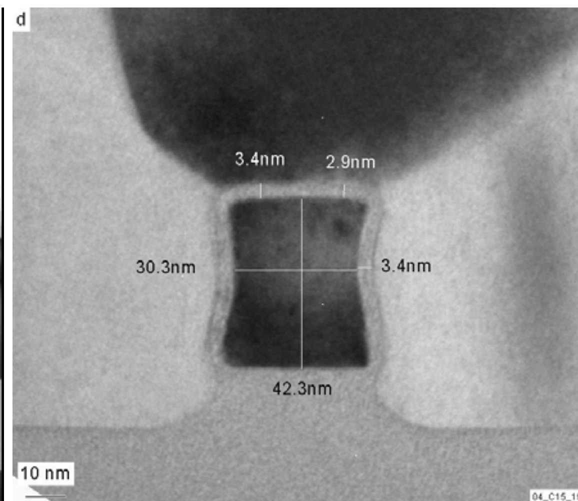

Figure 4: TEM cross section of a fin with height of 42nm and width of 30nm.

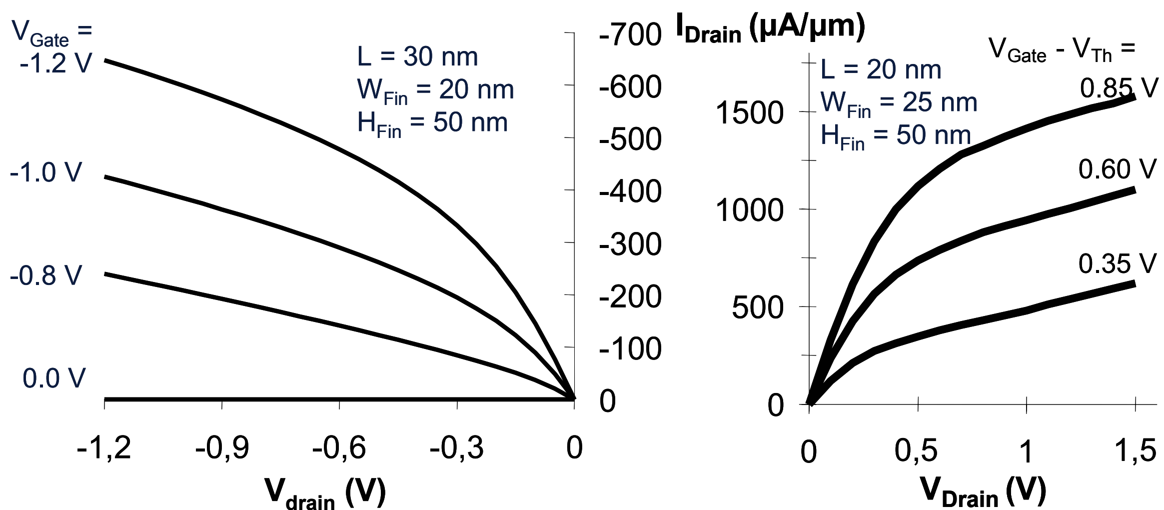

Figure 5: Output characteristics of a p-channel (left) FinFET (width of fin: 20nm, height: 50nm, gate length: 30nm) and an n-channel (right) FinFET (width of fin: 25nm, height 50nm, gate length: 20nm).