The MOS Single Electron Transistor (MOS-SET)

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We study very small gated SOI nanowires defined by e-beam lithography. Electrical transport at low temperature (below $\approx 10\,\mathbf{K}$) is dominated by Coulomb blockade. In the metallic regime at high V_g very periodic oscillations are recorded and the measured period corresponds to the whole surface of wire covered by the gate. Below the threshold the energy level quantization is clearly seen. The interplay between a charging energy and a mean energy level spacing of the same order of magnitude in a well controlled and characterized device is of great interest in view of making SET devices operating at room temperature. Indeed those devices have diameters below 10nm and are therefore in a regime where the energy level spacing cannot be neglected.

1 Device processing

Device fabrication is borrowed from SOI technology. Boron doped ($1\times10^{15}\mathrm{cm}^{-3}$) SOI (100) wafers are used. In order to ensure a low resistivity for the contact on silicon, the silicon film lying under the contacts is thick (70nm) and heavily doped. During its doping, the active areas are protected by a local thermal oxide in order to avoid amorphization of the thin underlying SOI layer. After the protection oxide removal, we proceed to ionic implantation of the thin active areas (above $\times10^{19}\mathrm{at.cm}^{-3}$). Their thickness ranges from 12 to 22nm. A hybrid DUV/Ebeam lithography combined with resist trimming is used to pattern silicon nanowires which sizes vary from 20 to 400nm. After silicon wire etching, a 4.5nm-thick gate oxide is thermally grown before CVD deposition of the in situ doped poly-Si gate. Ebeam lithography is then used to pattern gates down to 40nm. The back end sequence follows a standard CMOS process.

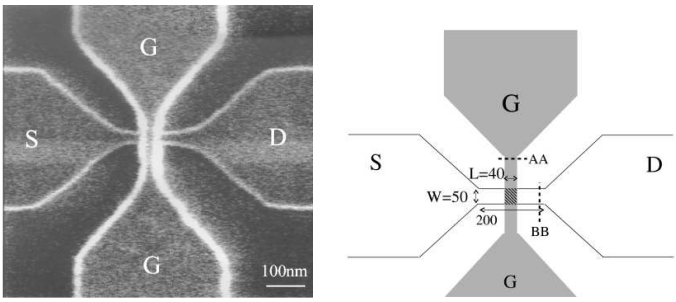

Figure 1: Left: Electron micrograph of the typical SOI gated nanowires studied in this work. For this particular device the width is W=50 nm, the wire length is Lf=200 nm and the gate length is Lg=40 nm. Right: schematic view with the cross section axis AA and BB along which the SEM pictures shown in figure 2 were taken.

Figure 2: Top: SEM image of the gate along the AA axis (see Fig.1), after resist trimming and etching. The gate length is 20 nm at its base. Bottom: SEM cross section of the wire along the BB axis.

2 Resistive confinement

Although most realizations of SET devices rely on tunnel barriers, it has been shown theoretically [2] and experimentally demonstrated [1, 3] that resistances also work, provided that their value is high enough, in fact larger than the quantum of resistance $R_K \approx 25.8\,k\Omega$. Our devices rely on this principle: the access resistance arising from the nanowire that is *not* covered by the gate provides the necessary impedance. Figure 3 shows the temperature dependence of a device. When the wire geometry and doping are well chosen the decrease of the saturation current with temperature is moderate and we observe several hundreds of perfectly reproducible resonances, as shown in Fig. 4. In the case where the access resistances are too high, they usually diverge with temperature and the resulting current through the device becomes too small. In the other extreme case of access resistances smaller than R_K, the saturation current increases with decreasing temperature but no Coulomb oscillations are recorder since confinement of the electronic wavefunctions is not provided.

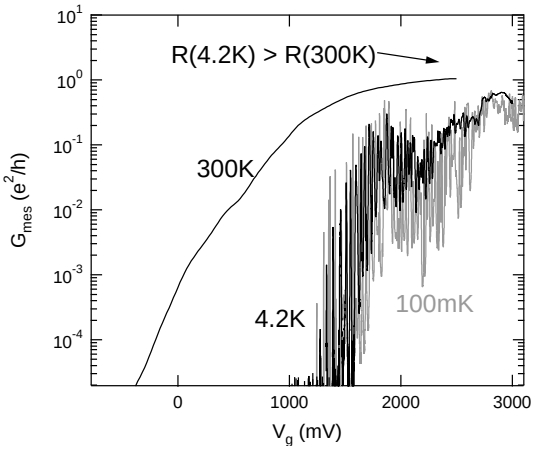

Figure 3: Temperature dependence of a 50x50x100 and 25 nm-thick sample, showing a very moderate decrease of the resistance at high V_g between 300 K and 4.2 K and very numerous (and periodic) Coulomb oscillations.

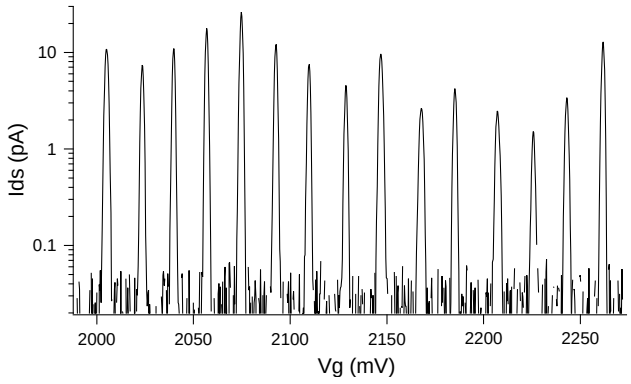

Figure 4: Id-Vg characteristics at very low temperature (100mK) for a WxLg=20x40 nm device, showing very periodic Coulomb oscillation with a high contrast. The film thickness is $\approx$ 17 nm. The measured period is $\approx$ 18 nm while the expected period considering the nominal size is 23.9 nm.

Figure 5 shows the so-called Coulomb blockade diamonds as we apply a finite V_{DS} larger than the very small bias usually used at low temperature to stay in the linear regime. These data are taken below the threshold, in the regime where the peak spacing fluctuates the most.

3 Geometrical control of the Coulomb oscillations

The measured period of the Coulomb oscillations ΔV_g can easily be compared with the expected period e/C_g, where the capacitance C_g is estimated from the nominal geometry of the gate/wire overlap and the planar capacitance of the gate oxide. This comparison, shown in Fig.6, yields a very good agreement. This shows that our quantum dots are defined by the gate/wire overlap, i.e. by etching, in contrast with $GaAs$ quantum dots formed by electrostatic depletion of split gates. This makes our devices original

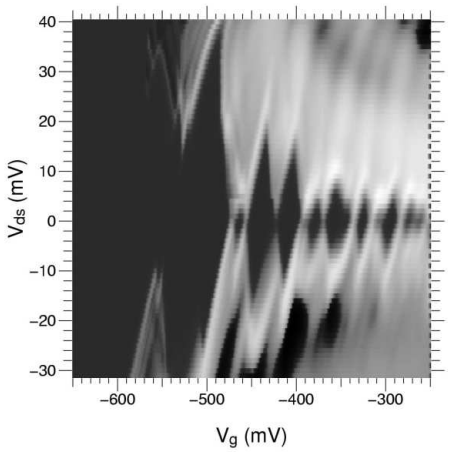

Figure 5: Finite-bias spectroscopy of a 30nmx30nm sample at 4.2K, showing diamond shaped structure characteristics of Coulomb blockade phenomena.

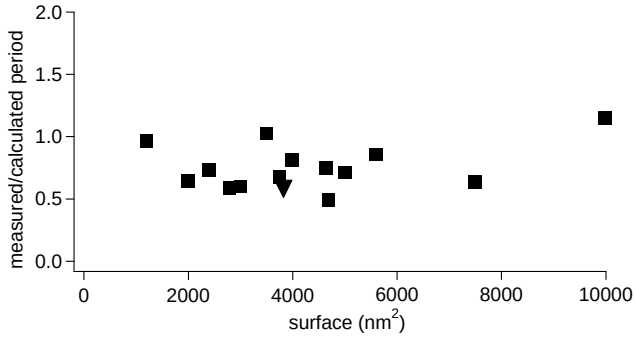

Figure 6: Ratio between the measured period and the period expected from the nominal gate/wire overlap for all the measured samples from different batches. The good agreement shows that the quantum dot is defined by lithography: its size is the nominal area of the gate/wire overlap.

tools to study the statistics of the mean level spacing when the size of the dot is small and constant [4], and also to study spin effects.

Conclusion

We have studied Coulomb blockade effects in gated SOI nanowires at low temperatures and show that our quantum dots are delimited by the size of the gate/wire overlap. This system is useful to study the physics of room temperature SET devices as well as fundamental properties of quantum dots such as the statistics of the addition spectrum and spin effects.

References

[1] V. A. Krupenin *et al.*, J. Appl. Phys., **90**, 2411, 1999.
[2] Y. Nazarov, Phys. Rev. Lett., **82**, 1245, 1999.
[3] X. Jehl *et al.*, IEEE trans. Nano., **2**, 308, 2003.
[4] M. Boehm *et al.*, in preparation.