QUANTUM TRANSPORT MODELING OF NANOSCALE MOSFETs

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Most aggressively scaled metal-oxide-semiconductor field-effect (MOSFET) transistors have characteristics dimensions entering now in the nanometer scale [1]. In this context, multi-gate nanowire MOSFET's are considered as the most promising candidates for ultimate CMOS integration, because of their efficient electrostatic coupling between the surrounding gate electrode and the conduction channel [2]. In the same time, strained-silicon channel devices, in which carrier velocity is enhanced via a strain-induced lattice deformation of the active layer (i.e. the conduction channel), also represent an emerging technological solution to enhance carrier transport in ultimate CMOS architectures.

This work surveys some of our recent results concerning the modeling and simulation of quantum transport of such nanoscale strained/unstrained devices. In a first part, we will introduce the fundamentals of the ballistic quantum transport through the study of a very simple system, i.e. an atomic chain double-gate MOSFET (Fig.1). We developed a mixed-mode simulation approach in which the electronic transport (belong the source-to-drain axis) is treated using the nonequilibrium Green's function formalism (NEGF) expressed in tight-binding and the electrostatic Poisson's equation is classically solved on a 2D domain [3]. Current-voltage characteristics and qualitative influence of point defect location on this ultimate device operation will be discussed.

In a second part of our presentation, we will detail how the NEGF formalism and the **k.p** theory [4] can be combined and used to study the theoretical ballistic operation of a strained silicon double-gate transistor (Fig.2) Our investigation shows that strain induced effects in very thin n-channel MOSFET is screened by the quantum confinement in the *z*-axis and then have a very limited impact on electron transport. On the other hand, the strain has a large influence on p-channel MOSFET. Considering the same off-current, our calculation predicts an enhancement of hole drive current of about 50% (Fig.3).

Finally, we will present some results concerning triple-gate and surrounding-gate MOSFETs which theoretically offer an enhanced gate control on the channel region (Fig.4). Simulation of these nano-transistors requires a full-3D quantum-mechanical treatment. We thus developed a numerical code separating the 3D Schrödinger equation into a 2D quantum confinement and a 1D quantum transport expressed in the NEGF formalism (Fig.5). Using this approach, we will illustrate some important results related to such mesoscopic systems, e.g. the notion of contact resistance associated to the potential drop in the electron reservoirs (Fig.6). We will compare the current-voltage characteristics obtained for different multi-gate structure and we will discuss the influence of the gate electrode architecture on device performance (Fig. 7).

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References:

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[2] J.P. Colinge, J.W. Park, W. Xiong, *IEEE Electron Device Lett.*, **24**, 515, 2003.
[3] M. Bescond, J.L. Autran, D. Munteanu, M. Lannoo, *Solid-State Electron.*, **48**, 567, 2004.
[4] S. Richard, N. Cavassilas, F. Aniel, G. Fishman, *J. Appl. Phys.*, **94**, 5088, 2003.

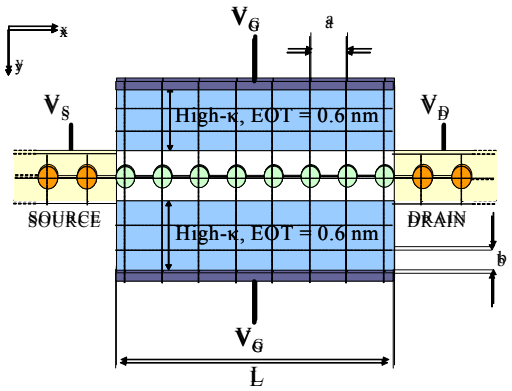


Fig.1: Single conduction channel double-gate MOSFET with metallic source and drain.

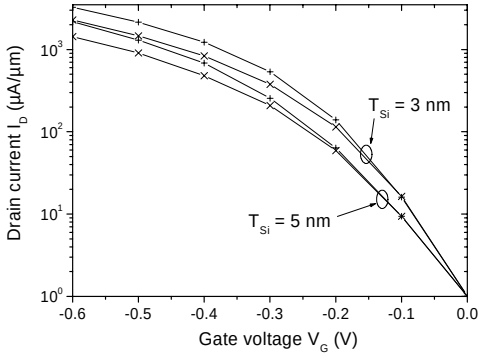


Fig.3: The calculated I_D-V_G characteristics for strained (+) and relaxed (x) p-channel with T_{Si} = 3 and 5 nm.

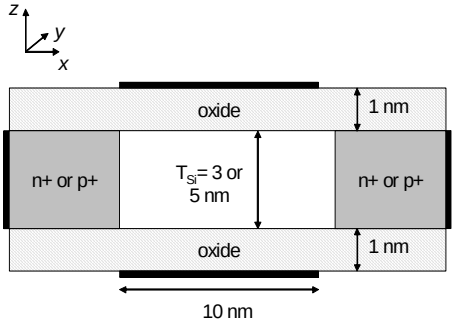


Fig.2: Schematic representation of a nanoscale double-gate MOSFET. The intrinsic channel is relaxed or strained with a tensile biaxial z-strain.

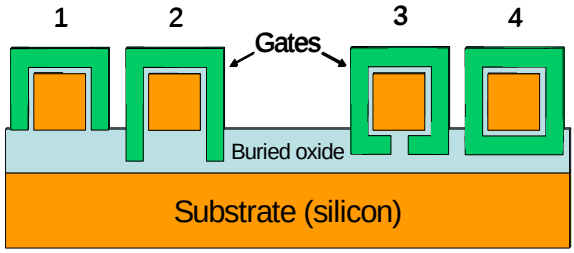
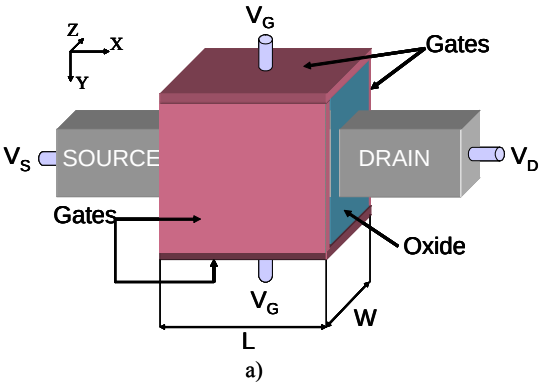


Fig.4: Cross-section of different gate configurations for nanoscale multi-gate transistors: 1) Triple-gate; 2) Π-gate; 3) Ω-gate; 4) Quadruple-gate (or Gate-All-Around structure).



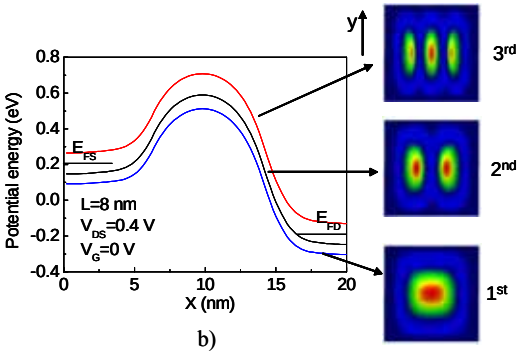


Fig.5: a) Schematic structure of the GAA (Gate-All-Around) MOSFET. The gates only surround the channel. For clarity, oxide layer is not represented around source and drain. b) First three subband minima along the transport direction of the GAA structure and their associated 2D square modulus of the eigenstate in a slice of the nanowire ((010) valleys).

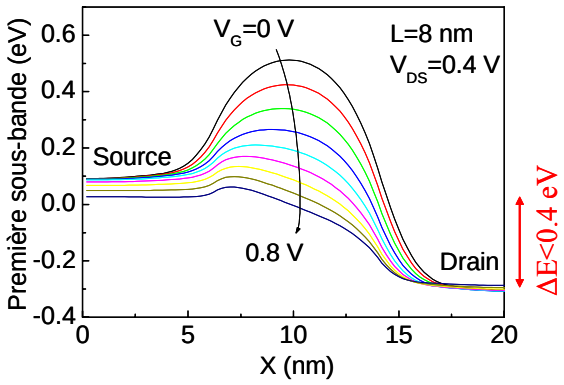


Fig.6: First sub-band evolution along the transport direction of the GAA structure for V_G varying from 0 V to 0.8 V by 0.1 V steps.

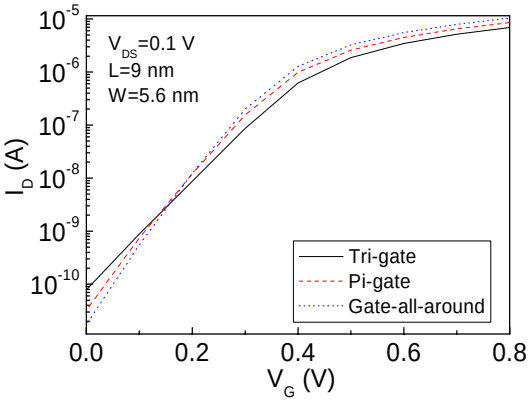


Fig.7: Comparison of I_D-V_G characteristics for three gate-structures.