Geometrical and electrical properties of ultrathin epitaxial metal nanowires on flat and vicinal silicon surfaces.

T. Block, S. Vagt, V. Zielasek, H. Pfnür
Institut für Festkörperphysik, Abteilung Oberflächen, Universität Hannover,
Appelstraße 2, D-30167 Hannover, Germany
e-mail: pfnuer@fkp.uni-hannover.de

Although the understanding of the conductive properties of extremely small metallic structures is of high importance for the potential use in nanoelectronic devices and their interconnects, the knowledge in general and the physical understanding of their properties is still rather incomplete. Quantization of electrical conductance has been demonstrated on metallic wires down to single atomic chains with a length of only a few atoms, which are suspended between electrodes in free space [1], using transmission electron microscopy and conduction measurements. However, the environment and its influence on the properties of metallic structures with a smallest extension in the nanometer range embedded in an insulating environment and connected to larger size contacts is still a problem barely addressed.

Here we present two methods to produce and study ultrathin epitaxial metallic nanowires. In the first, we combine electron beam lithography in ultra-high vacuum with epitaxy of silver on silicon (001) and (111) surfaces in order to generate crystalline metal nanostructures of arbitrary lateral shape with dimensions down to 10 nm on an insulating support. Our experiments are performed in a combined SEM-STM system (JEOL) for confocal and simultaneous operation of both microscopes at variable sample temperatures in the range 80-900 K. While the electron gun (1-25 keV) provides an SEM resolution of 4 nm a tiltable sample stage allows us to vary the angle of incidence between 30° and 0° so that also μRHEED images can be obtained.

Employing a nanolithography technique pioneered by Ichikawa and coworkers [2] we generate clean Si(001) or (111) windows, resp., within a thin thermal surface oxide layer of 0.3-0.7 nm thickness by means of electron-beam stimulated thermal desorption. After silver deposition at a sample temperature of 130 K we observe the nucleation of small Ag islands in the windows as well as on the oxide areas. At a sample temperature of 130 K we observe the nucleation of small Ag islands in the windows as well as on the oxide areas. As seen from Fig.1, subsequent annealing to room temperature or above leads to the formation of continuous flat epitaxial Ag wires with a minimal width of about 10 nm and a total length up to several micrometers that are constricted to the window areas, while spherical non-percolated Ag clusters with diameters of several nanometers form on the oxide areas.

Alternatively, we use Si(557) surfaces as templates that form regular arrays of triple steps between the terraces that are extended without defects over several hundred nm (see left part of Fig.2). Adsorption of several monolayers of Pb with subsequent annealing to temperatures above the melting point of bulk Pb leads to the decoration of the terraces by Pb nanowires with a typical width of 3 nm. Macroscopic conductivity measurements have revealed a remarably anisotropic (up to a factor of 20) conductance parallel and perpendicular to the step direction.

In order to determine the influence of single structural defects like grain boundaries, lateral constrictions, or atomic steps on electrical transport we generate the nanowires between TiSi contact pads that are produced on the substrate ex-situ via standard e-beam lithography. First measurements of electrical conductance of single crystalline Ag and Pb nanowires using the TiSi contact pads and the STM tip as probes will be presented.

References:

[1] H. Ohnishi, Y. Kondo, K. Takayanagi, Nature **395** (1998) 780.

[2] S. Fujita, S. Maruno, H. Watanabe, M. Ichikawa, J. Vac. Sci. Technol. B 16 (1998) 2817.

Figures:

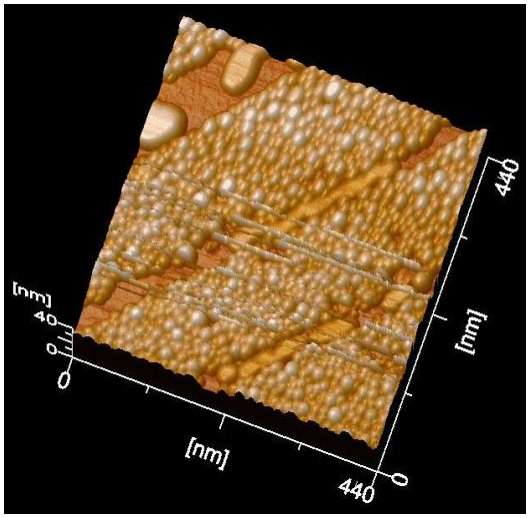

Fig. 1: STM image of Ag wires deposited into SiO_2 masks that are covered with non-contiguous Ag clusters.

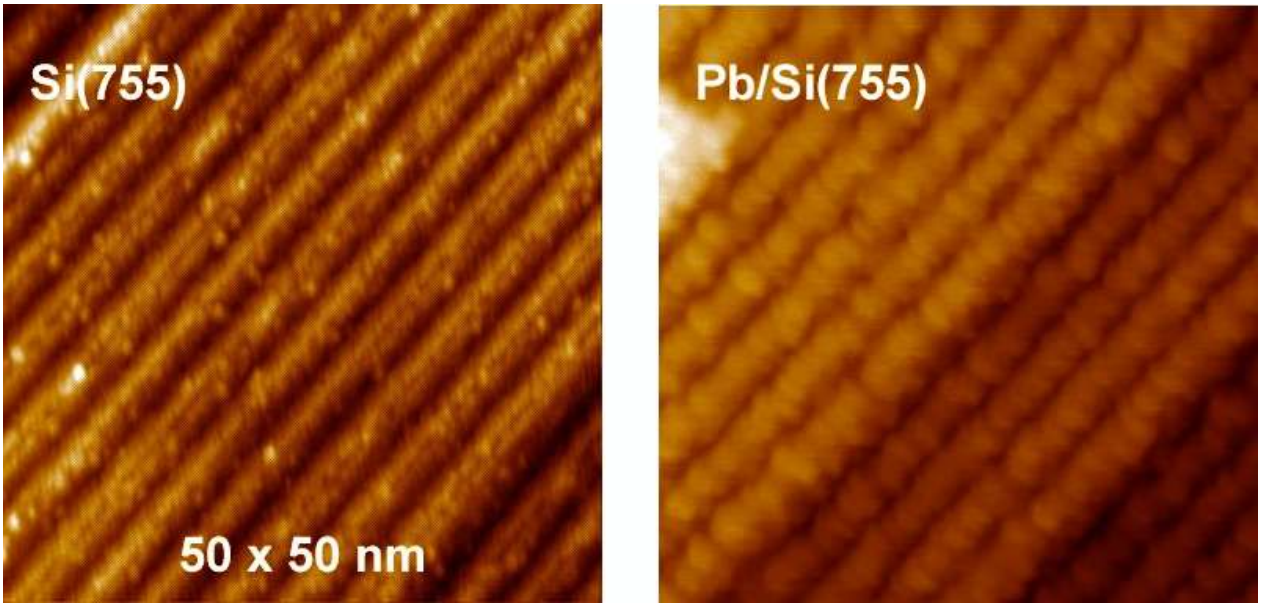

Fig.2: STM image of the clean Si(557) surface (left) and this surface covered with 5 ML of Pb after annealing to 620 K.