

SASEM

IST-2001-32674

**Self-Aligned Single Electron Memories
and Circuits**

Final Report

Covering period 01.01.2002-12.31.2004

DRAFT Version

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Project Co-ordinator: UCL

Partners: ISEN-CNRS-ST Microelectronics



**Project funded by the European
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Society Technologies”
Programme (1998-2002)**

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1 Executive summary

The SASEM project aimed at demonstrating single-electron memories and circuits for operation at room temperature as nano-flash memory devices.

The following table summarises the roles of the partners in the consortium.

Partner	Country	Role
UCL / Microelectronics laboratory	B	Process optimisation, device and circuits fabrication, characterisation, SOI circuit design, physical characterisation.
IEMN/ISEN	F	Process simulation and optimisation, lithography, device and circuits fabrication, physical characterisation.
ST Microelectronics	F	Characterisation (electrical and physical), benchmarking, prototyping

Year 1 has seen the achievement of all expected goals, mainly:

- Determination of best simulation tools given the peculiarities of the device: nano-scale object imbedded in a thick oxide.
- Optimization of process critical steps (nano-lithography, implantation, oxidation).
- High resolution imaging of low contrast Si/SiO₂ nanostructures.

Year 2 has built on this ground to move towards devices. The results showed clear advances, showing the feasibility of the objectives:

- Optimization of the process has been performed for a nano-dot of 15 nm in diameter that stores 10 to a few tens of electrons.
- Devices have been fabricated successfully based on the optimized process. Problems have been identified that do not originate from the optimized critical steps, but instead from larger scale steps.
- Characterizations show memory effect and very good reproducibility, as far as dot formation is concerned.

Following suggestions of the reviewers after year 2, the project has been re-focused on two targets:

- Transfer of critical steps on the industrial platform of partner ST.
- Down sizing of the memory device to go towards true single-electron behaviour. The objective was to scale down the initial device by a factor of 2. Simulations will target the feasibility of a factor of 4 down scaling.

Year 3 has seen the achievement of these two main goals.

- First, the bottleneck corresponding to the transfer of the “twin-nanowire” technology has been successfully lifted by the industrial partner (ST) in collaboration with the other partners. This was done by using classical process

tools, i.e. optical lithography, plasma etching and thermal oxidation. Beyond demonstration, improvements regarding etching profile and lithography will be important for process reliability.

- Memory devices with dots in the sub-10nm range (factor of 2 scaling down) have been fabricated successfully with a very high yield. The devices show signatures of single-electron effects at room temperature.
- Moreover, simulations tools are successful to predict formation of quantum dots in the nano-scale.

At the final term of the project, we can say that the SASEM project has fulfilled his objectives. The proposed technology has proved successful to fabricate single-dot memory devices by means of industrial process tools, and the same technology is suitable for further down sizing. While improvements are needed to go towards industrial implementation (lithography, etching, doping profile,...), the feasibility has been shown, and the use of quantum effects (Coulomb blockade and single-electron charging in our case) in practical devices was brought closer.

2 Project objectives

Future successful development of information technologies is strongly dependent on the continuation of Moore's law in the nano-electronics range. This imposes stringent constraints on the downsizing of semiconductor devices. From the 1999 ITRS roadmap, down-sizing of MOS transistors is known to be a major issue for the next few years as the technology will face a « brick-wall » near 2006 with no known solutions for the present CMOS technology in terms of dielectrics, doping, contact resistivity, ...

From the same roadmap, it appears that downsizing of memory devices turns out to be at least as big a challenge. For DRAMs, the main problem comes from the large capacitance needed to store the information in order to keep a low enough refresh rate (limited by the off-current of the associated MOSFET). In the last few years, downsizing of DRAMs was made possible thanks to complex geometry and exotic dielectrics that are hardly compatible with the mainstream MOS technology.

Integration of DRAMs with logic circuits is also a problem.

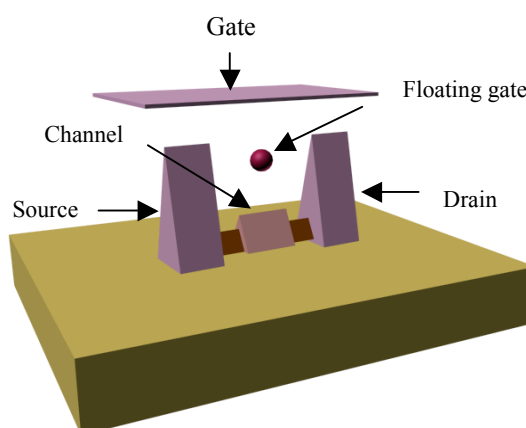
Flash memories also face downsizing problems mostly related to complex dielectric stacking and oxide degradation due to hot electrons (high voltage programming). However, their refresh free operation is interesting for low power applications. Low power devices are essential in order to reach ever-larger capacity memory circuits and enter portable equipments that will probably drive the next market revolution in electronics. According to most recent estimates, the « brick-wall » for both DRAMs and Flash memories is also around 2006.

Fundamentally, the above mentioned technological problems mainly originate from the fact that present devices are intrinsically hardly down-sizeable as their performances tend to deteriorate when sizes are reduced. It would be much more appropriate to turn to devices that benefit from downsizing. This is the case for single-electron devices, and, in the present context, single-electron memories (SEM), which make use of quantum effects which are strengthened by downsizing. In such devices,

a nano-meter scale floating gate is charged by one or a few electrons by making use of the energy quantization and Coulomb blockade effects. The induced electric field shifts the threshold voltage of the neighbouring MOS channel and the change in drain current is used to sense the charge in the floating gate. Because of the ultimately small amount of charge used for storage, the single-electron memory is the ultimate device for low power operation¹.

An ideal memory device for the coming nano-electronics era would be a silicon-technology compatible flash-like single-electron memory device. It would present the best performances in terms of integration, low power operation and future downsizing. The aim of this project is to fabricate and optimise such nano-flash single-electron memory devices and the associated circuits using a fully MOS-compatible silicon-on-insulator (SOI) technology.

Based on previous technology developments, partner CO1 as recently demonstrated a



new SOI single-hole memory device that operates at room temperature as a nano-flash memory. Figure 1 shows a 3D schematic view of the device. A silicon quantum dot is formed on top of a silicon channel and is embedded in the oxide that separates the poly-silicon gate from the channel. The gate and the channel form a SOI MOS p-type transistor. The dot is charged/discharged with holes by applying a negative/positive gate voltage to the gate. The persistent charge in the dot shifts the threshold voltage of the MOS transistor, which is used for readout. The main advantages of the device are low voltage and persistent programming. The process is self-aligned, completely MOS compatible, and requires only state-of-the-art optical lithography tools. Finally, the SOI technology is particularly well adapted as the device channel is confined as close as possible to the floating gate which ensures maximum shift in drain current on programming/erasing.

Figure 1: 3D schematic view of the single-electron nano-flash memory device

We have identified some critical points that currently limit performances: lithography resolution, process optimisation for improved reproducibility and better device operation, and fine characterisation. The objective of SASEM is to address these points and go from the existing laboratory SEM device to optimised device process

¹ « Mesoscopic physics and electronics », T. Ando et al. Eds., Springer 1998

and memory circuit demonstration. In order to fully exploit the potential of our SEM device, all aspects from physics and technology to circuit architecture will be addressed.

3 Methodologies

3.1 Innovation

The memory devices used up to now, in particular DRAM, face a technological brick-wall in terms of downsizing and operating frequency. Alternative memory devices/technologies are intensively investigated in order to provide next generation devices that will keep the future development of the microelectronics industry on the exponential track that allowed the booming of computer and communication technologies. The road towards the ultimate storage devices in terms of integration and low power, i.e. single-electron memories, has been paved by various technological schemes that present specific advantages. In SASEM, we propose a new self-aligned single-electron nano-flash memory device that combines the advantages of some of the foreseen technologies, but with significantly fewer drawbacks. Figure 1 (objectives) shows a 3D schematic view of the proposed single-electron nano-flash memory device. A nanometer scale silicon quantum dot is situated on top of a silicon channel and is embedded in the oxide that separates the poly-silicon gate from the channel (only the silicon is shown in Fig. 1). The technology proposed in SASEM starts from an SOI wafer and uses implantation of Arsenic to create a Gaussian profile of impurities in the active Si layer. The purpose of creating the As concentration profile is to tune the oxidation rate which is increased in the presence of As. In this process, the As concentration profile is so that the oxidation rate is maximum at some appropriate distance from the top of the silicon active layer. After defining the Si mesa by lithography and dry etching, wet oxidation is performed. Under appropriate conditions, the silicon wire (mesa) is separated into two wires (top and bottom) with silicon oxide in between. In this process, the width of the mesa wire is critical as one can go from only a bottom wire (narrow mesa) to two nanowires (intermediate size), and finally to a wide single wire. This tunability enables to create a quantum dot on top of a continuous channel by using a wide-narrow-intermediate-narrow-wide sequence. Figure 2 shows a simulation of the shape of the channel and quantum dot, while figure 3 shows a cross-section of the device where the quantum dot is situated between the triangular channel and the gate. The gate and the channel form a SOI MOS p-type transistor as Boron is used to dope source and drain. The dot is charged/discharged with holes by applying a negative/positive gate voltage to the gate, respectively. The persistent charge in the dot shifts the threshold voltage of the MOS transistor. The induced change in drain current is used for readout.

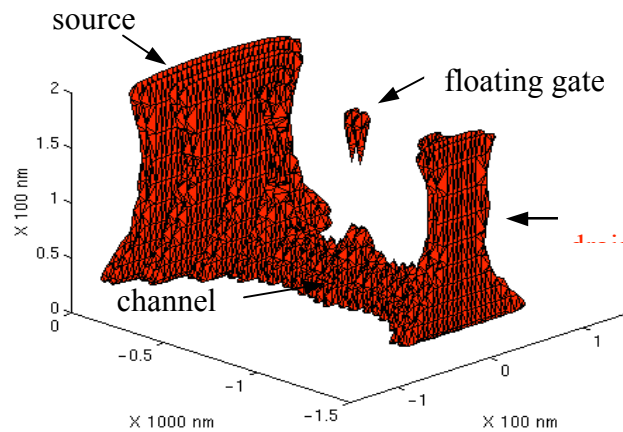


Figure 2: 3D stack along the channel length of 2D simulations that show the shape of the silicon channel and quantum dot that acts as a floating gate.

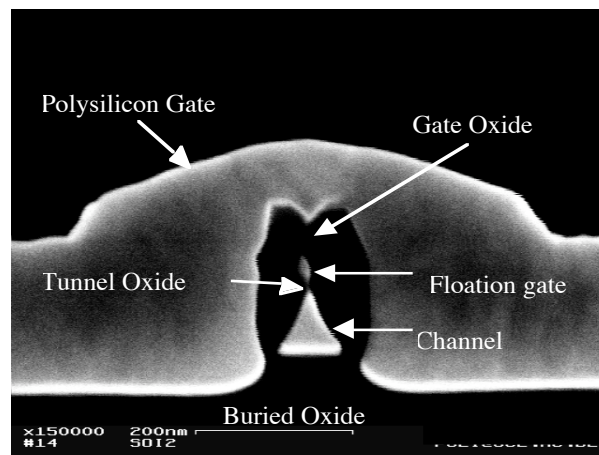


Figure 3: SEM image of the cross section of the central part of the device showing the quantum dot embedded in the gate oxide on top of the MOSFET channel.

3.2 Methodology

The methodology employed in SASEM groups the following ingredients:

- Process simulation using appropriate models for small devices and anisotropic oxidation. Wet oxidation, which is the key step in the proposed process, will be thoroughly investigated to provide a reliable simulation tool for process optimisation.
- Device simulation and design, and process optimisation for:
 - best reproducibility and robustness to process parameter fluctuations,
 - best device characteristics (Threshold voltage (V_T) and V_T -shift, gate leakage, programming/readout speed, retention time).
- Tests and optimisation of critical process steps, i.e. lithography and oxidation.
- Memory device fabrication with continuous feedback from physical characterisation and to device design.
- Physical characterisation (SEM, TEM, AFM, FIB).
- Electrical characterisation (programming and readout, transients, retention time...).

- Design and fabrication of memory cells (with programming/readout circuitry).
- Demonstration of a nano-flash single-hole 4x4 memory circuit.
- Analysis of feasibility at the industrial level and benchmarking.

3.3 Project plan and timing (Gantt chart)

The workplan schedule is summarised in the following timetable where the different workpackages are split into the different tasks described above.

Months	Year 1		Year 2		Year 3	
	1-6	7-12	13-18	19-24	25-30	31-36
WP0: management						
WP1: Design and simulation						
T 1.1 Process simulation tools						
T 1.2 Process optimisation						
T 1.3 Design of memory cell						
T 1.4 Design of memory circuit						
WP2: Fabrication						
T 2.1 Process steps optimisation						
T 2.2 Memory device fabrication						
T 2.3 Memory cell fabrication						
T 2.4 Memory circuit fabrication						
WP3: Characterisation						
T 3.1 Physical characterisation						
T 3.2 Development of characterisation tools						
T 3.3 Memory device characterisation						
T 3.4 Memory cell characterisation						
T 3.5 Memory circuit characterisation						

3.4 Comparison with other devices

The proposed device has recently been demonstrated for memory operation at room temperature and the measured or estimated characteristics are compared with those from other devices (Table 1) as obtained from the European 1999 MELARI roadmap for nanoelectronics.

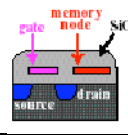
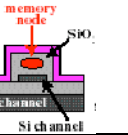
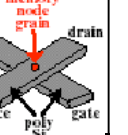
	Conventional Memory		Quantum Dot memory				
	DRAM	Flash	SET	Nano-flash			Yano
				Multi-dot	Single Dot	SASEM	
Device structure							
Read time	~10 ns	~10 ns	1 ns	~10 ns	~10 ns	~10 ns ²	~20 μs
Retention time	~1 s	~10 years	~1 s	~1 week	~5 s	>1 year ³	~1 day
Endurance cycle	∞	10 ⁶	∞	10 ⁹	10 ⁹	(single dot)	10 ⁷
Operating voltage	3 V	15 V	1 V	5 V	10 V	5 V	15 V
Logic-MOS process compatibility	no	no	Depends on material	Depends on material	yes	yes	yes
Lithography resolution	regular	regular	<2 nm	regular	<50 nm	regular	regular
Future down-sizing			✓	✓	✓	✓	✓
Electron number	10 ⁶	10 ³	1	10 ³	1	~10 ⁴	2
Cell size	~12 F ² /bit	~9 F ² /bit	~9 F ² /bit	~9 F ² /bit	~9 F ² /bit	~9 F ² /bit	2 F ² /bit

Table 1: Comparison of SASEM with other memory technologies. Red backgrounds indicate drawbacks from the various technologies, while green backgrounds indicate advantageous features for device fabrication, operation or future down-sizing. SASEM presents more advantages than any other reported technology for nano-memories.

The present device, even though not yet optimised, turns out to be a good candidate for future nano-memories as:

- it should exhibit fast readout time (SOI-MOSFET),
- it shows persistent charging,
- it uses relatively small operating voltages,
- it is totally MOS-compatible, including possible integration with logic circuitry,
- it can be manufactured using state-of-the-art optical lithography,
- it uses a self-aligned technology to produce the quantum dot and the channel simultaneously,
- it will benefit from future down-sizing (like other single-electron devices).
- it is intrinsically easy to scale down.

² Typical for a MOSFET transistor ; note that SOI presents even better frequency performances.

³ Lower limit extrapolated from the absence of decay for a two-days experiment.

⁴ Estimated from the observed shift in threshold voltage.

4 Project results and achievements

4.1 Overview of project results and achievements

Questions about project's outcomes	Number	Comments
1. Scientific and technological achievements of the project (and why are they so ?)		
<u>Question 1.1.</u> Which is the 'Breakthrough' or 'real' innovation achieved in the considered period	4	Brief description: 1. New process for elevated transistor and/or FinFet architectures. 2. Successful process simulation ready for downsizing device to real single electron memories. 3. Sub-10nm quantum dot self-aligned memory device compatible with MOS technology. 4. Technology transfer of a process realizing a nanoscale embedded quantum dot by means of regular MOS technology.
2. Impact on Science and Technology: Scientific Publications in scientific magazines		
<u>Question 2.1.</u> Scientific or technical publications on reviewed journals and conferences	Yes	10 publications (5 papers and 5 conferences) (see appendix for a complete list)
<u>Question 2.2.</u> Scientific or technical publications on non-reviewed journals and conferences	No	-
<u>Question 2.3.</u> Invited papers published in scientific or technical journal or conference.	Yes	2 invited papers and 1 invited talk
3. Impact on Innovation and Micro-economy		
A - Patents		
<u>Question 3.1.</u> Patents filed and pending	No	When and in which country(ies): Brief explanation of the field covered by the

		patent:
<u>Question 3.2.</u> Patents awarded	No	When and in which country(ies): Brief explanation of the field covered by the patent* (if different from above):
<u>Question 3.3.</u> Patents sold	No	When and in which country(ies): Brief explanation of the field covered by the patent* (if different from above):
Questions about project's outcomes	Number	Comments or suggestions for further investigation
B - Start-ups		
<u>Question 3.4.</u> Creation of start-up	No	
<u>Question 3.5.</u> Creation of new department of research (ie: organisational change)	No	
C – Technology transfer of project's results		
<u>Question 3.6.</u> Collaboration/ partnership with a company ?	Yes	Which partner : ST Microelectronics Which company : ST Microelectronics What kind of collaboration ? Project partner in characterization and fabrication
4. Other effects		
A - Participation to Conferences/Symposium/Workshops or other dissemination events		
<u>Question 4.1.</u> Active participation ⁵ to Conferences in EU Member states, Candidate countries / NAS.	Yes	SOI conference / Ukrain / March 2004 Invited plenary talk 3 other conference papers

⁵ 'Active Participation' in the means of organising a workshop / session / stand / exhibition directly related to the project (apart from events presented in section 2).

(specify if one partner or "collaborative" between partners)		
<u>Question 4.2.</u> Active participation to Conferences outside the above countries (specify if one partner or "collaborative" between partners)	Yes (1)	Names/ Dates/ Subject area / Country: MRS fall meeting/November 2004/US
B – Training effect		
<u>Question 4.3.</u> Number of PhD students hired for project's completion	1	In what field : nanoelectronics
Questions about project's outcomes	Number	Comments or suggestions for further investigation
C - Public Visibility		
<u>Question 4.4.</u> Media appearances and general publications (articles, press releases, etc.)		References: (Please attach relevant information)
<u>Question 4.5.</u> Web-pages created or other web-site links related to the project	Yes	References: http://www.dice.ucl.ac.be (Please attach relevant links)
<u>Question 4.6.</u> Video produced or other dissemination material		References: (Please attach relevant material)
<u>Question 4.7.</u> Key pictures of results		References: (Please attach relevant material .jpeg or .gif)
D - Spill-over effects		
<u>Question 4.8.</u> Any spill-over to national	No	If YES, which national programme(s):

programs		
<u>Question 4.9.</u> Any spill-over to another part of EU IST Programme	Yes	If YES, which IST programme(s): SINANO NoE
<u>Question 4.10.</u> Are other team(s) involved in the same type of research as the one in your project ?	Yes	If YES, which organisation(s): UCL

4.2 comparison to the original project objectives

While original objective was to make reproducible the process and transfer it to the industrial partner in the form of memory circuits, the decision was taken, after two years, to re-focus on process steps transfer, as well as further down sizing of the original device. This was motivated by the fact that the main point to solve regarding technology transfer was lithography, implantation, and finally wet oxidation. The rest is regular MOS process. Efforts by STMicroelectronics where targeted accordingly, and the critical technological steps where transferred successfully. Down-sizing has been motivated by the search for true single-electron behavior, again successfully achieved (factor of 2 down-sizing) thanks to strong efforts on lithography.

4.3 relations and synergies with other relevant projects

The research is continued within the NoE SINANO where single-electron effects will be studied intensively and further down-sizing pursued.

4.4 implications for EU policies and standards.

SASEM aims at demonstrating single-electron memory devices and circuits fabricated by means of a fully SOI-MOS compatible process. Therefore, the proposal aims to strengthen the European position in the microelectronics industry and keep up with the technology developments carried on in other continents, in the United States and in Japan where most of the work is currently performed. Even though Europe shares an important part of the world's microelectronics industry, the development of the "next generation" nanoscale memory devices as remained mostly non-European. The effort for a coherent development of the proposed technology requires the participation of research institutes with complementary domains of expertise. Partner UCL developed expertise in SOI circuit design and technology and runs a complete fabrication facility for SOI circuits (0.75 μm technology). On the other hand, partners IEMN and ISEN have expertise in process and device simulation, as well as high-resolution e-beam lithography and SOI processing. ST Microelectronics has leading-

edge skills in microelectronics technology, characterisation, benchmarking,... Obviously, the proposed work requires the combination of expertise from all the partners and hence needs to be done at the European level.

4.5 *benefits to society*

4.5.1 enhancing European competitiveness in a particular market

ST Microelectronics is a world leading company and a top actor in the European microelectronics industry. The participation of ST, which is interested in the high potential of the proposed technology, in this project will help strengthening the European position in this strategic business.

4.5.2 support the future growth of European industry;

The Information Society Technologies program yields “the development of an efficient networking and computing infrastructure together with advanced mobile and networked embedded systems that enable any-where/any-time access to services”.

The proposed work contributes to the above objectives by participating to the development of next generation memories that will enter virtually any electronic/communication equipment. The “user-friendliness” of the information technology will also benefit from this work as low-power, persistent, large capacity memories contribute to the easiness of operation, reliability and finally to the overall “confidence in the technology”.

SASEM addresses the rapidly growing microelectronics and telecommunication markets, where European companies have to compete on the global market. Thus, the high-volume production of memories and integrated logic/memory components will contribute to improve the employment in Europe.

4.5.3 protecting and preserving the natural environment and resources

SASEM aims at developing new single-electron memory devices. The smallest ever possible number of electrons, as well as the permanent storage of data, naturally favors low power applications which preserves natural energy resources.

The process used in SASEM is very close standard MOS process, and hence does not require the use of exotic materials.

4.5.4 the quality of life;

Portable applications like those allowing seamless communication, safe and easy transportation,... are favored by such low power devices.

4.5.5 employment within the European Union.

See 4.5.1

5 Deliverables and references

5.1 Deliverables

Deliverable No	Deliverable title	Delivery date (month)	Dissemination level
D1	1 st annual progress report	12	CO
D2	2 nd annual progress report	24	CO
D3	Final report	36	CO
D4	Report on process simulation tools	12	CO
D5	Report on optimised device process	24	CO
D6	Report on memory cell design	27	CO
D7	Report on memory circuit design	33	CO
D8	Report on critical steps optimisation	12	CO
D9	Report on device fabrication	27	CO
D10	Report on memory cell fabrication	30	CO
D11	Report on memory circuit fabrication	36	CO
D12	Report on device characterisation	30	CO
D13	Report on memory cell characterisation	33	CO
D14	Report on memory circuit characterisation	36	CO

5.2 Main deliverables

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°: 5 – Report on optimized device process

Due date: December 31, 2003

Delivery Date: December 31, 2004

Short Description:

Deliverable D5 reports all the investigations made following D4 and the 1st year report on process steps optimisation. All the different tunable ingredients have been investigated in order to find the best stability conditions for the formation of the storage quantum dot. The output of D5 was used to fabricate devices and device arrays. The first edition of D5 has been updated according to the additional work performed during the third year, in agreement with the reorientation of the project approved by the scientific officer after year 2 review.

Partners owning: IEMN

Partners contributed: IEMN-ISEN

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°6: Report on memory cell design

Due date: March 2004

Delivery Date: December 2004

Short Description:

The design of memory cells, best suited for the SASEM device, is presented and discussed in this deliverable.

Partners owning: ISEN

Partners contributed: UCL

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°7: Report on memory circuit design

Due date: September 2004

Delivery Date: December 2004

Short Description:

The read/write array circuit designed for exploitation of the SASEM device is presented in this deliverable. The different options are discussed in view of the specific characteristics of the memory device.

To realize the final circuit, select transistors must be performed altogether with memory devices.

This deliverable reports on fabrication and characterization of elevated source drain MOSFET.

Partners owning: ISEN

Partners contributed: UCL

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°9: Report on device fabrication

Due date: March 2004

Delivery Date: December 2004

Short Description:

This deliverable sums the results obtained during the SASEM project regarding device fabrication.

Partners owning: UCL

Partners contributed: UCL-STMicroelectronics

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°10: Report on memory cell fabrication

Due date: June 2004

Delivery Date: December 2004

Short Description:

The fabrication of memory cells his reported in this deliverable.

Partners owning: UCL

Partners contributed: UCL-ST Microelectronics

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°11: Report on memory circuit fabrication

Due date: December 2004

Delivery Date: December 2004

Short Description:

Following the second project review, the project has been refocused on technology transfer of critical steps (partner ST) and on the study of scaled down devices in order to reach single-electron behaviour (UCL-CNRS-ISEN partners). The memory cell contribution was set aside until these two prior issues were solved. Consequently, while the fabrication of memory cells was performed and reported in the second year report and in D10, fabrication of memory circuits could not be performed as the two major issues took all our efforts till the end of the project. The present deliverable could therefore not be filled, in agreement with the decision taken by the project officer and the reviewers of the project.

Partners owning: UCL

Partners contributed: UCL

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°12: Report on device electrical characterisation

Due date: December 2004

Delivery Date: December 2004

Short Description:

The present deliverable sums up the work performed device electrical characterization during the SASEM project.

Partners owning: UCL

Partners contributed: UCL-STMicroelectronics

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°13: Report on memory cell characterisation

Due date: September 2004

Delivery Date: December 2004

Short Description:

Following the second project review, the project has been refocused on technology transfer of critical steps (partner ST) and on the study of scaled down devices in order to reach single-electron behaviour (UCL-CNRS-ISEN partners). The memory cell contribution was set aside until these two prior issues were solved. Consequently, while the fabrication of memory cells was performed and reported in the second year report and in D10, electrical characterization could not be performed as the two major issues took all our efforts till the end of the project. The present deliverable could therefore not be filled, in agreement with the decision taken by the project officer and the reviewers of the project.

Partners owning: UCL

Partners contributed: UCL-STMicroelectronics

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°14: Report on memory circuit characterisation

Due date: December 2004

Delivery Date: December 2004

Short Description:

Following the second project review, the project has been refocused on technology transfer of critical steps (partner ST) and on the study of scaled down devices in order to reach single-electron behaviour (UCL-CNRS-ISEN partners). The memory circuit contribution was set aside until these two prior issues were solved. Consequently, while the fabrication of memory circuit arrays was performed and reported in the second year report and in D10, electrical characterization could not be performed as the two major issues took all our efforts till the end of the project. The present deliverable could therefore not be filled, in agreement with the decision taken by the project officer and the reviewers of the project.

Partners owning: UCL

Partners contributed: UCL-STMicroelectronics

Made available to: reviewers

DELIVERABLE SUMMARY SHEET

Project Number: IST-2001-32674

Project Acronym: SASEM

Title: Self-Aligned Single Electron Memories and Circuits

Deliverable N°15: Report on physical characterisation

Due date: December 2004

Delivery Date: December 2004

Short Description:

This deliverable presents a few highlights of the work performed in SEM characterization during the SASEM project. The rest of the work is disseminated all along the other deliverables as well as in the periodic reports.

Partners owning: UCL

Partners contributed: UCL-STMicroelectronics

Made available to: reviewers

5.3 Publications in books and journals

- X. Tang, X. Baie, J. P. Colinge, Member, IEEE, C. Gustin, and V. Bayot, Two-Dimensional Self-Consistent Simulation of an SOI Nano-Flash Memory Device with a Triangular P -Channel, *IEEE Transactions on Electron Devices*, Vol. 49, No. 8, pp. 1420-1426, August (2002).
- X. Tang and V. Bayot, Silicon Single-Electron Memories, *Belgian journal of electronics and communications*, *HFrevue* No. 3, pp. 17-26 (2002). (**invited review paper**)
- X. Tang, N. Reckinger and V. Bayot, Fabrication of SOI Nano Devices, NATO ASI Series, NATO Advanced Research Workshop, Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment, edited by Denis Flandre, Alexei and Peter Hemment (**invited paper**).
- C. Krzeminski, E. Dubois, X. Tang, N. Reckinger, A. Crahay, V. Bayot, « Simulation et optimisation d'une mémoire flash nanométrique », *Proceedings GDR Nanoélectronique* (2004) in press
- C. Krzeminski, E. Dubois, X. Tang, N. Reckinger, A. Crahay, V. Bayot, «Optimisation and Simulation of a alternative nanoflash memory: the SASEM device», , *Proceedings MRS Fall meeting* (2004) D1.6

5.4 Conferences

- X. Tang, N. Reckinger and V. Bayot, SOI Nano Device Fabrication, oral presentation at NATO Advanced Research Workshop, Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment, which was hold on 25-29 April, (2004), in Kyiv, Ukraine (**invited talk**).
- C. Krzeminski, E. Dubois, X. Tang, N. Reckinger, A. Crahay, V. Bayot “Simulation et optimisation d'une mémoire flash nanométrique », *Journées nationales GDR nanoélectronique*, Aussois, Mai 2004, (Oral communication)
- C. Krzeminski, E. Dubois, X. Tang, N. Reckinger, A. Crahay and V. Bayot; “Optimisation and Simulation of an Alternative Nano-flash Memory: The SASEM Device”, 2004 MRS (Materials Research Society) Fall meeting, (Oral communication).
- X. Tang, N. Reckinger, V. Bayot, E. Dubois, C. Krzeminski “Self-aligned single-electron memories: towards single-electron operation of MOS compatible nano-flash memory devices”, *Sinano workshop*, Grenoble, January 2005, (Oral communication)
- X. Tang, N. Reckinger, V. Bayot, E. Dubois, C. Krzeminski, A. Villaret, D. Bensahel “Self-aligned single-electron memories”, *NID workshop*, Madrid, February 2005, (Oral communication)

6 Future outlook

The following table summarises the benefit of the partners in the consortium.

Partner	Benefit
UCL	Optimization of the twin-nanowire technology. Enhanced reproducibility. Prediction tools for complex nano-scale 3D patterning of silicon films. Nano-lithography.
IEMN/ISEN	Process simulation and optimisation. A powerful process simulation tool is now available to investigate complex geometries involving gradients in doping and long oxidations.
ST Microelectronics	Characterisation (electrical and physical) of nano-scale quantum dot devices, twin-nanowire technology available for future devices.

7 Conclusions

To be completed after the review meeting.