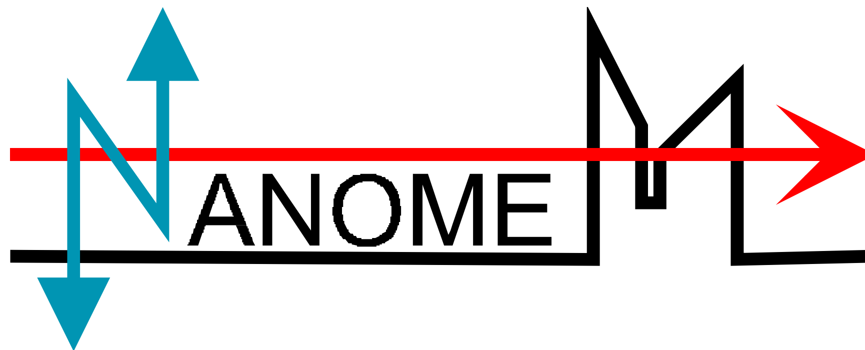
Semiconductor Free Nanoscale Non-Volatile Electronics and Memories based on Magnetic Tunnel Junctions



IST–1999-13471

Semiconductor Free Nanoscale Non-Volatile Electronics and Memories based on Magnetic Tunnel Junctions

Final report

Report Version: 1

Report Preparation Date:

Classification: confidential

Contract Start Date: 1st January 2000 Duration: 44 month

Project Co-ordinator: UHP, Nancy - Pr. Alain Schuhl

Partners: ULP, Strasbourg; MAGOX, Oxford; SIEMENS, Erlangen; Thales, Orsay

Project funded by the European Community under the "Information Society Technologies" Programme (1998-2002)

Table of Contents

Page	
3	**I - Executive summary**
5	**II – Management of the project**
5	**II-1 Project objectives**
6	**II-2 Methodology & management**
10	**III - Project results and achievements**
10	**III-1 Overview of the progress of the project**
10	**III-1.1 Project starting point**
13	**III-1.2 At mid term**
18	**III-1.3 At this end of the project**
32	**III-2 Main milestones**
34	**III-3 Main deliverables**
39	**III-4 Comparison to the original project objectives**
39	**III-5 Relations and synergies with other relevant projects**
39	**III-6 Benefits for European Society**
41	**IV - Future Outlook**
44	**V - Information dissemination and exploitation of results**

I - Executive summary

First commercialization of Magnetic Random Access Memories (MRAM) based on magnetic tunnel junctions (MTJ) will probably concern embedded memories. Leaders in the industry of electronics such as Motorola or IBM/ Infineon have already announced for the end of 2003 a commercial MRAM device. Independent non volatile MRAM will probably enter in the market during the end of a next year. The first generation will definitely consist in a combination of magnetic tunnel junctions as storage elements and CMOS transistors for avoiding the parasitic cross-talk between the elements in the memory array matrix. However, the limitation of this concept concerns the cell size which is determined by the lateral size of the transistor. In already available demonstrators, the surface of the unit cell is of the order of 25 F^2 , where "F" is the smallest size achievable with the technology used. It corresponds usually to the lateral size of the tunnel junction.

In the framework of this state of the art, the main contribution of the NanoMEM project was to determine the validity of semiconductor-free components in the second generation of magnetic memories, which would have the advantage of decreasing both the cells size and the fabrication costs. Two different approaches have been followed in parallel, respectively Metal-Insulator-Metal Random Access Memories (MIMRAM) and Three Terminal Random Access Memories (TTRAM) devices. In contrast to the first generation of MRAMs, the proposed MRAMs do not contain CMOS transistors to prevent the parasitic signal paths through metal lines and tunnel junctions. However, a critical element to prevent the above parasitic effect is to obtain a sufficiently strong current asymmetry ratio within the tunnel junction element, combined wit a high magneto-resistive ratio.

This report presents the main progresses within the NanoMEM project. During all the period of the project, the work was pursued on both devices evoked in the NanoMEM initial proposal: MIMRAM end TTRAM. The project has been successful in disclosing a number of novel and interesting phenomena and processes related to the evaluation of the feasibility of MRAMs of a second generation.

As far as the MIMRAM are concerned, individual Metal-Insulating-Metal (MIM) structures as fundamental elements of MRAM have been experimentally elaborated. They show a promising current asymmetry ratio of 200. This important result, makes from the MIMRAM the first device without semiconductors with such a such large current asymmetry/blocking ratio. Moreover, this result match the initial objective of the NanoMEM project (asymmetry ratio 200/1). In parallel to the experimental work intensive numerical modeling has been performed. These studies have shown that the MIMRAM asymmetry ratio can still be experimentally improved by optimization of the structural properties of the multi-layer stack and by a proper choice of insulating barrier parameters. Moreover, in order to improve the MIMRAM magneto-transport characteristics, intensive work has been performed in order to clarify the fundamental origin of current asymmetry and variation of the TMR with applied voltage. Experimentally, in the last step of development, the MIM has been integrated in a full MIMRAM. In a single integrated structure, current asymmetry and tunnel magneto-resistance (TMR) was measured.

As far as the TTRAM are concerned, even at the end of the project, the development of the TTRAM devices still confronts with technological problems. The main difficulty

originates from the electrical contact in the middle electrode and the damaging of the top and bottom tunnel junctions during the patterning steps. However, despite of these technological problems, the TTRAM device is theoretically predicted to have the highest magneto-current asymmetry, so the best magneto-transport / blocking properties in a MRAM matrix array. Over all the extension of the project, the origin of the technological problems related with the middle contact have been intensively studied. Therefore, the damaging of the bottom tunnel junction has been definitely reduced during the junction device patterning steps. Nevertheless, at the end of the project we still confront with technical problems for TTRAM realization. A low-voltage breakdown of the bottom junction still occurs, after the junction patterning process. Moreover, the top tunnel junction of the TTRAM stack seems to be damaged during the patterning steps, even if in a simple junction architecture this junction works properly. Concerning the optimization of the magneto transport response of the TTRAM device, alternative magnetic electrodes have been studied to eliminate the parasitic magnetic couplings effects between the three magnetic electrodes. From a theoretical point of view, over all the extension of the project, a numerical code has been developed to compute the TTRAM magneto-electrical characteristics. This code represents a very useful tool for optimizing, prior to the experimental elaboration of the multilayer stack, the best choice of material parameters for the magnetic materials and the insulators. Therefore, we have shown that that the best configuration consists in a magnetic emitter and base. No significant effect of a magnetic collector has been shown. Nevertheless, a magnetic collector is useful to assert the integrity of the top tunnel junction. Finally, a first SPICE model of the TTRAM has been made and the first read/write protocols have been studied.

In parallel to the studies concerning materials and technological processing, an important amount of time has been allocated to optimize the architecture of the auxiliary electronics in order to make a fast and reliable reading of the information stored in the RAM array. This experimental setup was followed by a computation model which predicts the highest RAM size that can be addressed depending on the MIM current asymmetry ratio.

On the basis of the main results of the NanoMEM, project one can conclude that both lines, MIMRAM and TTRAM devices should be taken into account for future developments.

II – Management of the project

II-1 Project objectives

Contemporary computer information storage has several shortcomings. Firstly, the active memory (mostly DRAM, Dynamic Random Access Memory) is volatile, dissipates large amounts of energy owing to the need for frequent refreshing and occupies much space owing to the requirement that each memory cell incorporates a capacitor. Secondly, background storage on hard-disk has large access times and almost unacceptably high mechanical failure rates owing to the information being read by sensors positioned close to a rapidly rotating magnetic disk. With projected increases in data storage densities and transfer rates, this technology is set to become decreasingly acceptable.

With these considerations in mind, it is likely that the future of computing will be dominated by the use of non-volatile Magnetic Random Access Memory (MRAM). This consists of arrays of individual magnetic memory cells in which the information is stored as the magnetisation direction of tiny ferromagnetic elements. Writing these elements uses a multiplexed current pulse technique to reverse selected magnetic elements, and the read process relies on tunnelling giant magneto-resistance. The characteristics of these MRAM memory cells offer a winning combination of high speed, low power, non-volatility, large density, low cost and no moving parts. Moreover, in contrast to virtually all other aspects of the computer industry, the basic science behind this new technology was born in Europe, and thus offers the first real opportunity for European dominance in this highly competitive, fast-moving and lucrative market.

The **overall thrust** of this project was to demonstrate the feasibility of **two new varieties** of Tunnelling-MRAM, **MIMRAM (Metal-Insulator-Metal RAM)** and **TTRAM (Tunnelling Transistor RAM)**, in order to demonstrate their capability to replace the currently available generation of RAM (which is based on semiconductor technology) in all applications is clearly measurable.

Compared with other Tunnelling-MRAM architectures, the **MIMRAM (two terminal)** and **TTRAM (three terminal)** concepts offer the advantage of small cell size and hence high packing density, in conjunction with suppression of parasitic signal paths in read and write operations.

Let us recall the specific objectives of the initial project :

Objective 1 Eliminate the current bottleneck on reducing the size of MRAM cells, i.e. the space taken up by the blocking diode or transistor, by implementing MIMRAM (where the blocking is done by a MIM diode of dimensions equal to the memory cell size) and TTRAM (where the spin - transistor itself performs the blocking function). This allow the length-scale of MRAM cells to be reduced from 0.35 to 0.1 micron.

Objective 2 Reduce the impedance of the smaller MIMRAM and TTRAM cells (without inducing tunnelling hotspot problems due to thinner insulator layers) by implementing tunnelling barriers of lower height. Smaller tunnelling RAM

cells imply higher electrical impedance and hence longer read time since the integrating capacitor of the read circuitry is fixed.

Objective 3 Choose materials and fabrication methods to maintain switching fields at the same level and accuracy when the magnetic elements are reduced from 0.35 microns to 0.1 microns. Reducing the size of MRAM cells causes an increase in the size and scatter of magnetic switching fields. This in turn implies larger magnetisation currents and higher power dissipation. The NanoMEM methodology is to remove extraneous sources of magnetic anisotropy by employing very thin films of low magneto-striction material in an AAF (artificial anti-ferro-magnet) construction and by imposing tighter control over the lithographic shapes.

Objective 4 Adopt fabrication procedures which suppress the parasitic conduction paths arising due to the signal from the smaller MRAM cells being more susceptible to contamination from edge conduction effects round the periphery of the tunnel junction.

Objective 5 Model and implement solutions aimed at increasing the spin dependent signal of the MIMRAM and TTRAM cells such as spin enhancing quantum interference and spin–selective barriers. Access times and reliability of the MRAM cells are a function of signal-to-noise ratio.

Objective 6 Reduce of the influence of cross-talk by the implementation of a 3×3 matrix addressing protocol for read write operations which imposes cancelling signals to reduce incidence of signal errors due to such cross-talk. Cross-talk between the magnetic elements and/or the control lines of adjacent memory cells is a problem which is exacerbated by higher packing density.

Objective 7 Develop of reliable fabrication procedures for realising the necessary hardware and the development of a working read/write protocol. Implementation of TTRAM requires the use of three separate sets of control line arrays and a special pulse read protocol in which DC bias voltages are used to suppress the parasitic conduction paths and the signals are written and read as superimposed voltage pulses.

II-2 Methodology & management

After two years, both concepts have been demonstrated. The main point was the important increase of the blocking function of the two solutions for a second generation of MRAM. Current asymmetries, *a*, above 20 have been demonstrated in TTRAM, and above 200 in MIMRAM and cells. We also already observed simultaneously blocking function and magnetoretistance on the same device. These results represented an important progress as compared with the state of the art when the project started (a=1.3). The comparison between experimental results and modeling allowed to validate our model of transport and put in perspective the possibility to increase the *a* asymmetry up to more than 10^4.

Let us point out here the difficulties, which appeared during the second year, after important changes in the consortium:

- ✓ First, one of the partners, MPG of Halle, did not could hire people in order to produce is part of the work program. This did not leaded to important problems, since is tasks have been done by two partners, mainly ULP and also UHP.

- ✓ Second, some important part of researchers and also of materials moved out from the partner ULP which was in charge of the high frequency part of the work program. Since no one is the consortium have the facilities to produce these experimental job, we had to stop the corresponding progress. However, looking to the state of the art progress, we are convinced now that the solution for solving the micromagnetism problems that could occurs at high frequency are already available in the literature. Moreover the concept on which this project is based, the MIMRAM and the TTRAM, do not introduce specific difficulties when looking for the high frequency aspect. So we believe that we can achieve the final device of the project with the actual knowledge based on first generation of MRAM.

In their report written after the Catania review meeting, the referees present a similar analysis. On one hand, the report evaluates as overestimated the initial objective of the project. "In the course of the two years in which the project has been running, a gap seems to have been developed between the initial objectives and those that can be perceived as feasible at the present time. For this reason, we consider that a reappraisal of the specific goals of the project and schedule is most needed." On the other hand, the referees emphasize on the importance of the progresses obtained during the first two years. " The scientific work carried so far has already achieved considerable progress. A variety of alternative materials for spin-selective electrodes were investigated. Studies on different shapes of sub-µm-MTJ for MRAM were carried out. Sub-µm-MTJ were fabricated and investigated. Alternative barriers for MTJ and for a maximum TMR were investigated. The blocking functionality that has been attained in the devices is a significant step forward. For the first time such diode-like behaviour in a magnetic system was demonstrated. The blocking ratio achieved is of the factor of 40. Design aspects were investigated showing that the achieved blocking behaviour is still far away from a minimum specification. The blocking has to be increased up to 10^4 in order to avoid effectively parasitic currents in a MRAM-array. Simulations show that 10^5 are theoretically feasible. "

Following the referees report and our own analysis of the status of the progresses as compared to the objectives we have proposed:

- to concentrate on the proof of both concepts surveyed: the TTRAM and the MIMRAM concepts, followed by the fabrication of the memories matrix. Consequently, the deliverables in the remaining part of the project are:

- ✓ A significant increase in the blocking ratio.
- ✓ A working single cell (TMR + blocking).
- ✓ A TTRAM or MIMRAM matrix.

to postpone the end of the project for 6 months, namely up to the end of June 2003, in order to put enough efforts on the main bottlenecks and to increase of the blocking ratio by more than one order of magnitude.

During the second half of the project, we then pursued the work on both devices evoked in the NanoMEM initial proposal. On one hand, some aspects of the technological problems with the Three Terminal Random Access Memories have been solved and a current of hot electrons could be observed. A current asymmetry of 40 was measured even if no spin polarisation was detectable. From the theoretical point of view, this device is however predicted to have the highest magneto-current asymmetry. On the other hand, the Metal-Insulator-Metal Random Access Memories (MIMRAM) showed an experimental current asymmetry of 200, 10 times more than the state of the art reported after 18 months of work inside the consortium. Furthermore, a TMR signal was reported when an additional tunnel junction was grown on top of the diode.

Since the project included an important number of scientific teams. Our co-ordination between the partners has been based on a day-by-day management of the scientific progress of the research, and the rapid circulation of the information within the consortium. The Steering Committee, comprising one technical manager from each partner, did meet at least three time each year in order to oversee the evolution of the progresses total project. The Steering committee insured the achievement of the milestones and the completion of the deliverables.

City	Type of meeting	date
Pisa	NID meeting	Feb 2000
Nancy	Steering+Workgroups	Apr 2000
Paris	Steering+Workgroups	Oct 2000
Barcelone	NID meeting	feb 2001
Oxford	Steering+Workgroups	Sept 2001
Strasbourg	Steering+Workgroups	Jan 2002
Catania	NID meeting	Feb 2002
Erlangen	Steering+Workgroups	Oct 2002
Paris	Steering+Workgroups	mars 2003
Cork	NID meeting	Juin 2003

Main meeting of the steering committee and of the workgroups

The project was divided into six main Work Packages including for each of them the Work Package leader and a technical representative of the partners involved in the Work Package. After the redefinition of the work program, the number of Working group have been reduced

to three. These Working Groups did **meet at least two times per year**. Two of the meetings being held linked to the six monthly meetings of the Steering Committee.

Collaboration

The second action of the management team has been devoted to the develop an increasing collaboration between partners during the all contract period. A large number of samples did travel trough all Europe. Focussing on the last 18 month we have obtained an important number of sample travel between different partners. For example, the partner Thales did patterned the devices on structures grown by Siemens and ULP, while the structures of both MIMRAM and TTRAM was discussed conjointly by the steering committee. Samples did travel from Orsay (Thales) and Strasbourg (ULP) to Nancy (UHP).

Main objective	Type of collaboration	Partner	Partner	Partner
MIM-RAM	Samples	ULP	Thales	
	Samples	ULP	Siemens	
	Modelisation	ULP	UHP	
TTRAM	Samples	UHP	Thales	Siemens
Matrix	Demonstrator	Siemens	Oxford	
	Modelisation	Siemens	Oxford	

Rapid overview of the main collaboration during the last 18 month

III - Project results and achievements

III-1 Overview of the progress of the project

III-1.1 Project starting point

A Magnetic Random Access Memory (MRAM) consists of arrays of individual magnetic memory cells in which the information is stored as the magnetisation direction of tiny ferromagnetic elements. Writing these elements uses a multiplexed current pulse technique to reverse selected magnetic elements, and the read process relies on tunnelling giant magneto-resistance. The characteristics of these MRAM memory cells offer a winning combination of high speed, low power, non-volatility, large density, low cost and no moving parts. Moreover, in contrast to virtually all other aspects of the computer industry, the basic science behind this new technology was born in Europe, and thus offers the first real opportunity for European dominance in this highly competitive, fast-moving and lucrative market.

The overall thrust of NanoMEM is to develop two new varieties of Tunnelling-MRAM (Magnetic Random Access Memory) based on two terminal devices MIMRAM (Metal-Insulator-Metal RAM) and three terminal devices TTRAM (Tunnelling Transistor RAM). The objective of this proposal is to develop this new technology to the degree where it is capable to replace the currently available generation of RAM (which is based on semiconductor technology) in all applications.

The MIM diode

The purpose of using a MIM (Metal-Insulator-Metal) diode in the memory cell is to prevent parasitic conduction through neighbouring cells during the read process. Consider the schematic array of memory cells shown in Figure 1. In order to address the cell labelled A the signal is passed between the read lines I and II. Parasitic conduction can occur through a number of paths via neighbouring memory cells, one such being shown by the heavy line in the figure. In order to eliminate these extraneous contributions to the signal, it is proposed to block all other possible paths by making use of the fact that the parasitic currents all pass through at least one cell in the reverse direction. Thus by integrating a diode into the memory cell these can be eliminated.

The use of a MIM diode rather than a semiconductor diode will allow the minimum size of the cells to be determined by the size of the magnetic tunnel junction rather than the size of the diode. The principle of the MIM diode can be seen by considering the energy level diagrams shown in Figure 2.

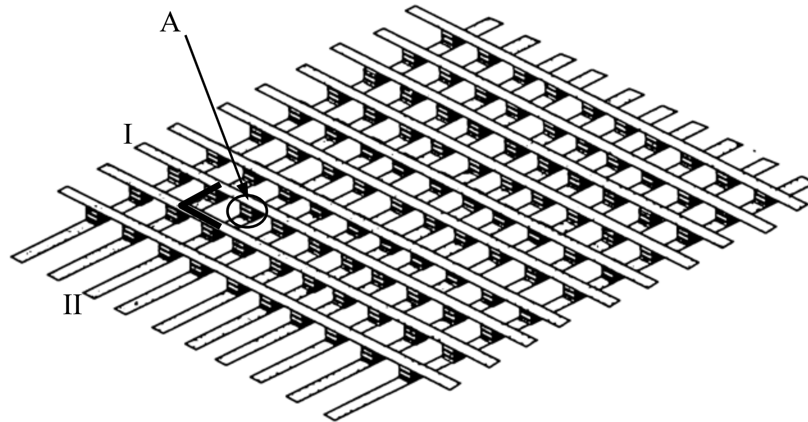


Fig.1 - Array of memory cells

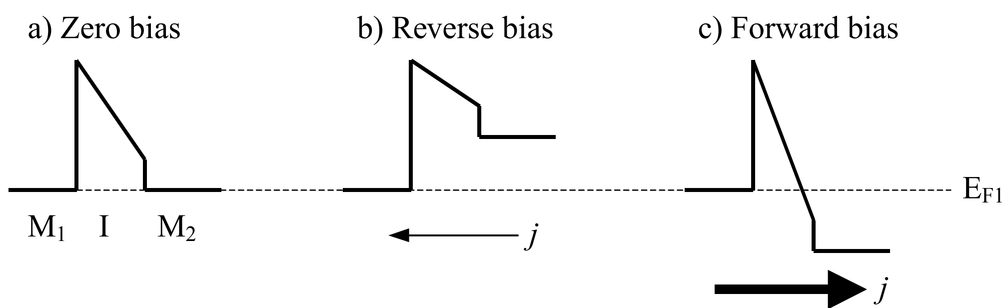


Fig.2 - Schematic energy level diagram of MIM diode under different bias conditions

The asymmetry in the behaviour of the diode under forward and reverse bias is due to the difference in the work functions of the two metals. Current flow across the diode is due to tunnelling of electrons through the insulating layer. In the forward biased case the average height of the barrier is seen to be lower than in the reverse case and the tunnelling probability (and hence the current flow) is therefore larger. The limiting factor in the potential performance of a MIM diode is the difference in the work functions of the two metals. In order to achieve a high degree of asymmetry in the conductance curve it is therefore desirable to use metals with highly different work functions. This is an aspect of the fabrication which we will be intensively studying during the course of the NANOMEM contract.

However, considering the work functions of different metals, current asymmetries less than 1.3 could be measured experimentally. At this stage, the NANOMEM contract found oneself in a dilemma. An other architecture had to be found.

Transistor application of Three Terminal Devices

The TTRAM consists in a double magnetic tunnel junction (MTJ) in which an electrical contact is taken on each of the three metallic electrodes. One of the MTJ is used as the storage element, whereas the other acts as a filter of the ballistic current, which is directly travelling from the emitter to the collector. The two operating conditions of the TTRAM as a memory element are summarised in figure 3. If the element is not intended to be read, the MTJ between base and collector is reverse biased ($V_{bc}<0$). Consequently, a negative current I_c is observed, which reflects the tunnelling of electrons from the collector into the base (I_c is the collector current). No ballistic current is observed. If now the memory element is intended to be read, this same MTJ has to be forward biased ($V_{bc}>0$). In that case, a positive I_c collector current is observed, which corresponds to the superimposition of the tunnelling current between base and collector and the ballistic current from the emitter to the collector, which is now allowed to travel. This ballistic current contains the stored information to be read.

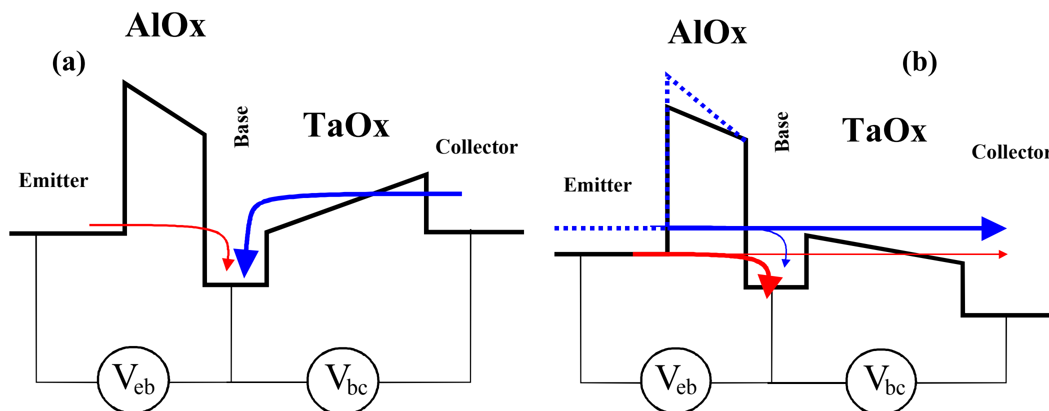


Fig. 3 - Scheme of operation of the TTRAM as a MRAM memory element. (a) the element is not intended to be read (switch off) ; (b) the element is intended to be read (switch on).

Such a TTRAM used as a memory element has thus two main figures of merit. First of all, the asymmetry of the characteristics I_c vs. V_{bc}, which measures the ability for the system to differentiate the opened situation from the closed one. The second figure of merit is the dependence of the ballistic current intensity with the magnetic configuration between the emitter and the base (parallel or antiparallel) and also collector (if needed). It measures the ability to differentiate a '0' from a '1' information.

For this device, several bottleneck had to be solved :

- **We need in a single structure tunnel barriers with different barrier heights (so a need for two barrier materials)**
- **We need three magnetic materials with three different coercive fields**
- **We need to take an electric contact in a layer with thickness less than 10 nm.**

III-1.2 At mid term

During the first half of the project, we have shown that the material growth bottleneck has been removed since two 'working' tunnel junctions (before technological steps) with different barrier heights and materials have been stacked. Furthermore, the coercive fields of the magnetic electrodes are different (1600, 400 and 50 Oe) and allow the stabilisation of different magnetic configurations and so to the TMR measurement of each tunnel junction.

MIMRAM

The work has then progressed very rapidly for the MIMRAM technology because it uses the well established technological steps optimised for conventional tunnel junctions. The new concept of asymmetric double junction MIMIM structure depicted in figure 4 has been investigated. This new concept exploits the combination of the asymmetry of the potential profile and the coherent electronic transport in multiple (double) barrier metal/insulator systems. The concept exploits also the possibility of *adjusting the asymmetry of the potential profile by the choice of each barrier*, see figure 4. This constitutes an additional degree of freedom for tuning the asymmetry ratio of the diode current-voltage characteristics.

Beyond an 'intrinsic' asymmetry expected for the I(V) characteristics, related to the asymmetric potential profile of the two barriers configuration, the asymmetry can be 'enhanced' by two main features of electron tunnelling in the metal / insulator quantum well system:

a) Hot electron transport

   For forward voltage, if the voltage drop V_1 on the first barrier is larger than the second barrier height U_2, the electrons become hot for the second barrier (figure 4.-c). Therefore, in terms of tunnelling, they experience only the first barrier and the corresponding tunnel current is high. For backward voltage, for the opposite voltage drop on the two barriers, the electrons experience both barriers (figure 4.-d). Therefore a high asymmetry ratio between the currents corresponding to the forward and backward voltage $\mathbf{A = Ic^f/Ic^r}$ is theoretically expected.

b) Coherent / incoherent resonant tunnelling (related to the quantum well located in between the two insulating barriers)

   When the electrons tunnel coherently, a strong enhancement of the current asymmetry ratio is expected. This resonant associated enhancement can be explained in a simple model, assuming one resonant energy level located in the quantum well.

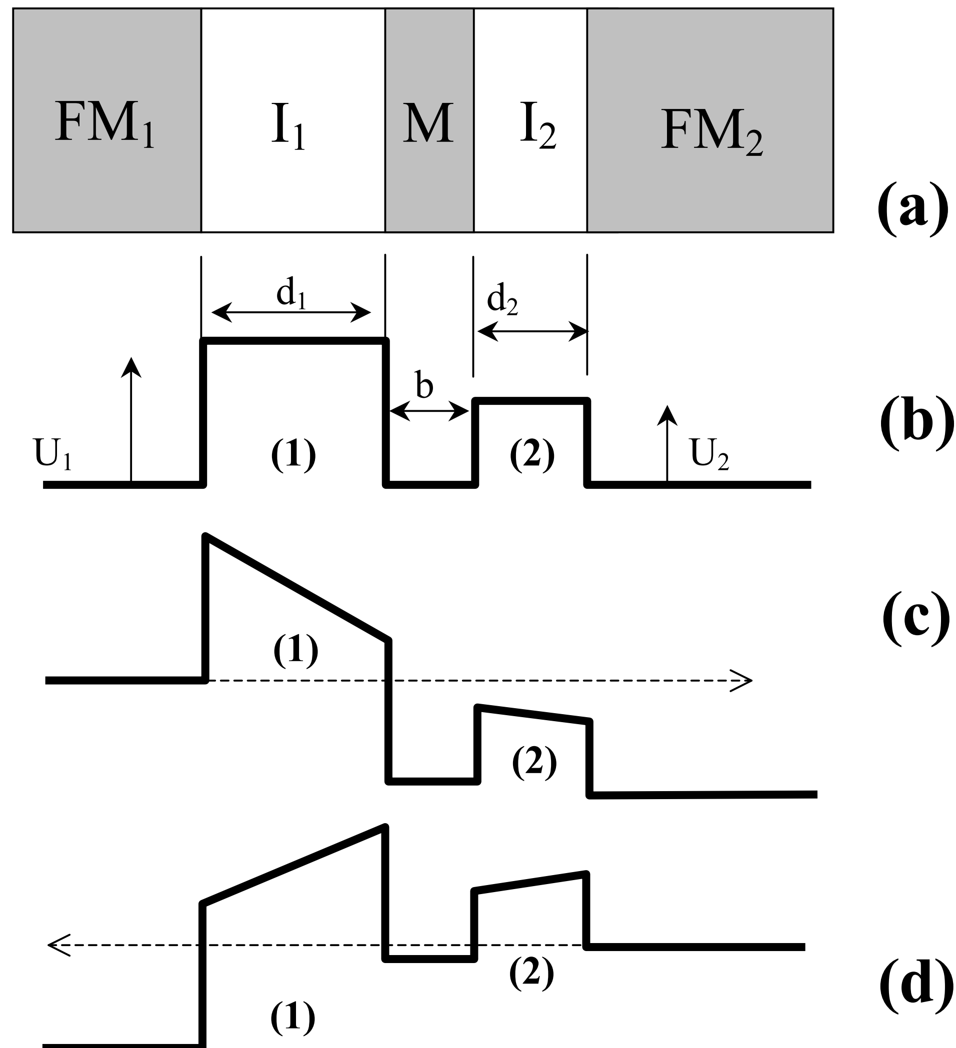


Fig. 4 - Asymmetric potential profile in a double barrier system. (a) Sketch of the multilayer MIMIM structure (b) associated potential profile where U_i and d_i are the potential height and the thickness of the i-th barrier, (c) with a positive applied voltage (forward) and, (d) with a negative applied voltage (backward)

Double barrier tunnel junctions have been elaborated [by sputtering, in the following standard multilayer configuration: Substrate / buffer layer / **FM_1 / I_1 / M / I_2 / FM_2/** capping, where:

- Substrate : naturally oxidized Si (Si/SiOx)
- Buffer layer: Cr(1.6nm) / Fe(6nm) / Cu(30nm)
- Bottom (magnetic) electrode (FM_1): / CoFe(3nm)
- Top (magnetic) electrode: (FM_2) Co(6nm)
- M = metallic middle layer of Cu
- I_1, I_2 = insulating Al_2O_3 barriers

According to the simulations, the **hot electron transport criteria** may be achieved if the barrier parameters are chosen properly, in order to favour the voltage drop across one of the barrier and therefore to inject the hot electrons across the second barrier. In this purpose, the

first barrier is chosen to be thick and to have a high barrier height and the second one thin and having a small barrier height.

These requests are verified in the following configuration:
- **I_1 = Al_2O_3** of estimated barrier parameters **d_1 =1.5nm, U_1 =2.3eV**
- **I_2 = Al_2O_3** of estimated barrier parameters **d_2 =1nm, U_2 =0.8eV**

A maximum of the asymmetry ratio is observed for the system where the metallic interlayer is discontinuous. Corresponding to this system, for an external voltage of 1V the asymmetry ratio of the current voltage characteristics is slightly higher then 20. As illustrated by figure 5-a, the asymmetry ratio increases monotonously with the external voltage, reaching a maximum value whose origin is a direct proof for the presence of the resonant state in the metallic quantum well.

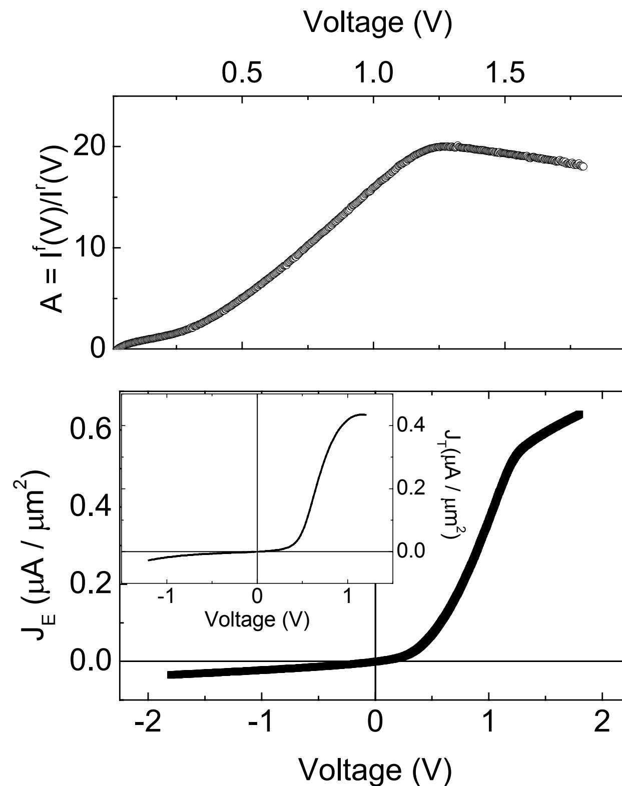


Fig. 5 - (a) Variation of the asymmetry ratio with the external voltage. (b) I(V) characteristic of MIMIM double barrier system. Inset : theoretical curve, expected for coherent resonant tunneling in double barrier system.

This maximum value corresponds to a maximum value for the forward current reached when the energy of the electrons injected across the first tunnel barrier reaches the resonance level. In the current - voltage characteristic (figure 5-b) this maximum corresponds to the kink measured on the positive branch of the *I*(*V*) curve, around 1V. Interestingly, as illustrated on the inset of figure 5-b the experimental *I*(*V*) characteristic matches perfectly to the theoretical expectation, calculated in the framework of the quantum mechanical model.

Extremely important for potential applications of the MIM double barrier diode is not only the large asymmetry but also the variation of the asymmetry with the external voltage. Indeed, as illustrated by figure 5-a, by varying the external voltage around the value corresponding to the maximum value we preserve a large asymmetry ratio for a voltage range of 1V +/- 0.5 V.

In 18 months, a major breakthrough concerned the current asymmetry which was brought from 1.3 to 25. Unfortunately, even with the use of magnetic materials, no TMR signal could be observed in the MIM structure. This is in accordance with simulations. Indeed, they show that when electron tunnelling resonance occurs, the TMR signal decreases.

TTRAM

During the first half of the project, we have shown that tantalum oxide prepared by plasma oxidation of sputter-deposited tantalum is a suitable material for low barrier height spin dependent tunnelling devices. Magnetoresistance ratios of 4% are easily obtainable by the choice of a suitable Ta thickness and oxidation time. The material exhibits low barrier heights of around 0.4eV. This is of particular importance for the TTRAM working. The work has progressed more slowly for the TTRAM technology than for the MIMRAM because the development of the technology used to realise the electric contacts appeared as a major technology bottleneck. The difficulty to stop the ion etching in a thin metallic layer has been circumvent by the use of an Auger spectrometer in a first step and then with the use of a SIMS spectrometer.

The double barrier tunnel junctions has to be elaborated with two tunnel junctions of different barrier heights in the same stack. The typical stack of such double barriers is as follows :

substrate/Ta/$Co_{80}Fe_{20}$/Co/**Al_2O_3**/Py/**TaO**/Co/Ta

where
- The float glass substrate has a smooth surface.
- The following 10nm thick Ta layer is a buffer to erase the glass substrate scratches
- The magnetic electrodes are made with a $Co_{80}Fe_{20}$(7.5nm)/Co(2nm) bilayer for the bottom electrode, a Py(xnm) layer for the middle electrode and a Co(20nm) layer for the top electrode.
- The Al_2O_3(1.5nm) and TaO(3nm) tunnel barriers are made by the subsequent oxidation of as deposited Al(1.2nm) and Ta(1.2nm) metallic layers
- The Co top electrode is capped by a 10nm thick Ta layer to prevent from oxidation.

The characteristics of each tunnel junctions could be measured using the electric contact which has to be taken on the base electrode.

The $Co_{80}Fe_{20}$/Co/$\mathbf{Al_2O_3}$/Py bottom tunnel junction

As we can see in figures 6 and 7 (left), the bottom tunnel junction presents a characteristic non linear current/voltage curve and a tunnel magneto- resistance signal of about 15%. Furthermore, the coercive fields of the $Co_{80}Fe_{20}$/Co and Py electrodes, of about 400 and 50 Oe, are different enough to ensure a well defined antiparallel magnetic state. The resistance of this junction is about 80 kΩ and its surface is 110×75 μm^2.

The Py/**TaO**/Co top tunnel junction

As we can see in figures 6 and 7 (right), the top tunnel junction presents a characteristic non linear current/voltage curve and a tunnel magneto- resistance signal of about 4%. Furthermore, the coercive fields of the Co and Py electrodes, of about 1600 and 50 Oe, are different enough to ensure a well defined antiparallel magnetic state. The resistance of this junction is about 420 kΩ and its surface is 50×50 μm^2. **The top stacked TaO tunnel junctions keep their characteristic (barrier height of about 0.5eV, TMR of about 4%) even when grown on a previous $Co_{80}Fe_{20}$/Co/Al_2O_3/Py tunnel junction.**

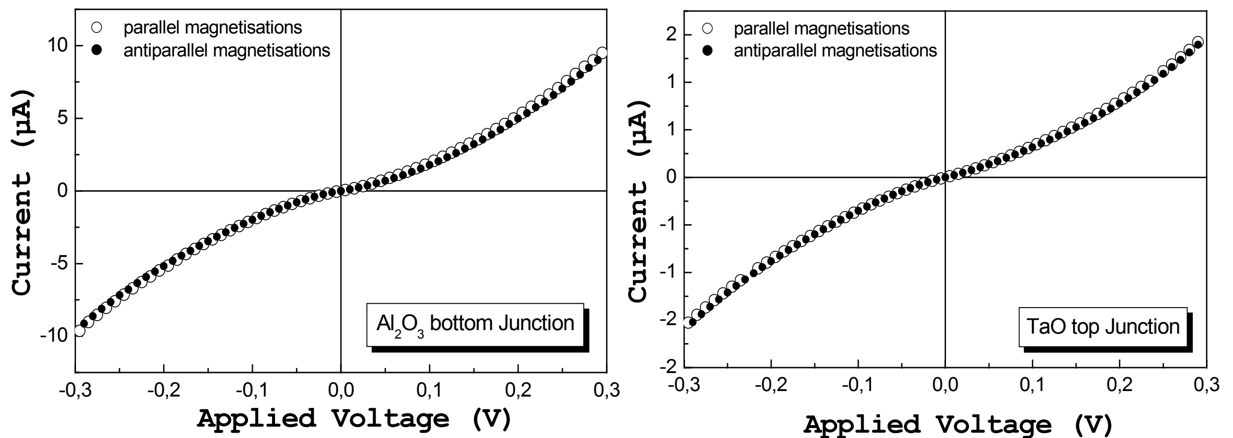


Fig. 6 - Characteristic current/voltage curves measured at 77K on the Al_2O_3 (left) and the TaO (right) tunnel junction which compose the TTRAM cell.

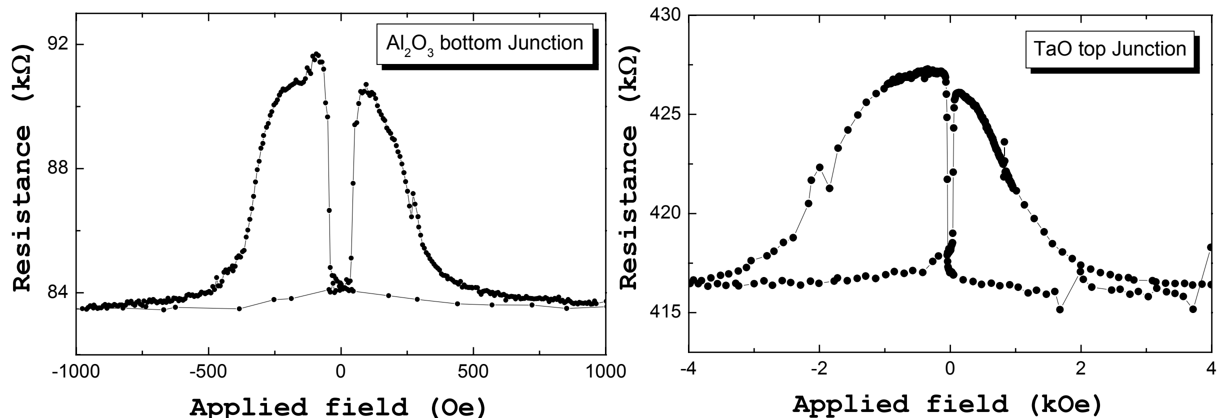


Fig. 7 - Characteristic resistance/magnetic field curves measured at 77K on the Al_2O_3 (left) and the TaO (right) tunnel junction which compose the TTRAM cell.

In the light of those results, the material growth bottleneck has been removed since two 'working' tunnel junctions with different barrier heights have been stacked. Furthermore, the coercive fields of the magnetic electrodes are different (1600, 400 and 50 Oe) and allow the stabilisation of different magnetic configurations and so to the TMR measurement of each tunnel junction.

No proof of hot electron transmission has been given at this stage. We have shown that etching the top barrier induces defects in the bottom barrier. We expect to solve this problem with the use of the new neutralised ion beam etching source.

In 18 months, a major breakthrough concerned the growth of a TTRAM with magnetic field dependent tunnel characteristics. Unfortunately, no hot electron spin dependent current could be observed.

III-1.3 At this end of the project

During the second half of the project, we pursued the work on both devices evoked in the NanoMEM initial proposal. On one hand, some aspects of the technological problems with the Three Terminal Random Access Memories have been solved and a current of hot electrons could be observed. A current asymmetry of 40 was measured even if no spin polarisation was detectable. From the theoretical point of view, this device is however predicted to have the highest magneto-current asymmetry. On the other hand, the Metal-Insulator-Metal Random Access Memories (MIMRAM) showed an experimental current asymmetry of 200, 10 times more than the state of the art reported after 18 months of work inside the consortium. Furthermore, a TMR signal was reported when an additional tunnel junction was grown on top of the diode.

III-1.3.a - MIMRAM

We have significantly increased the asymmetry ratio of the MIM diode using Al as the intermediate metallic layer instead of Cu. This choice was motivated by the clustered growth of Cu onto the Al oxide which is hard to control. In order to get a more continuous intermediate metallic layer, we have partially oxidise a thin Al layer deposited onto the first Al oxide one. We have then obtained large asymmetries on a few junctions (see figure 8) of a same wafer. We conclude that this system is certainly the best choice for the MIMRAM since it gives us more reproducible I-V curves with high asymmetries more than 10 times larger than the samples containing Cu.

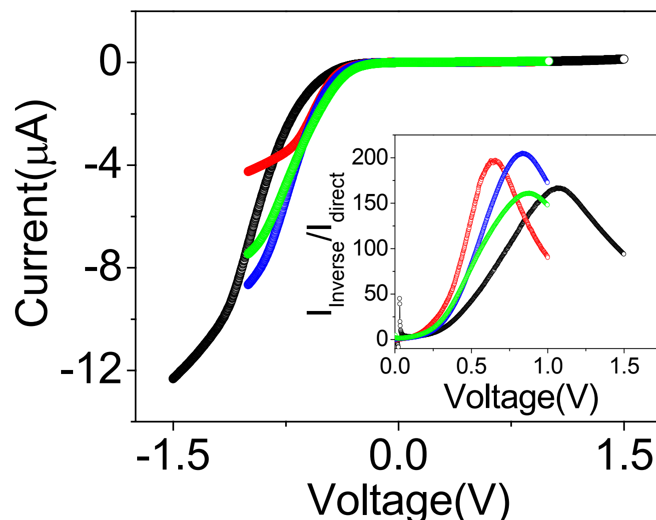


Fig. 8 - I-V curves with high asymmetries more than 10 times larger than the samples containing Cu

We have patterned the first MIMRAM junctions by adding a single magnetic tunnel junction onto the previously developed MIM diode (figure 9). In this system, the hard layer consist in a thick CoFe layer and the soft layer consist in a thinner Fe layer : the AAF is then useless and helps only for the growth of the diode.

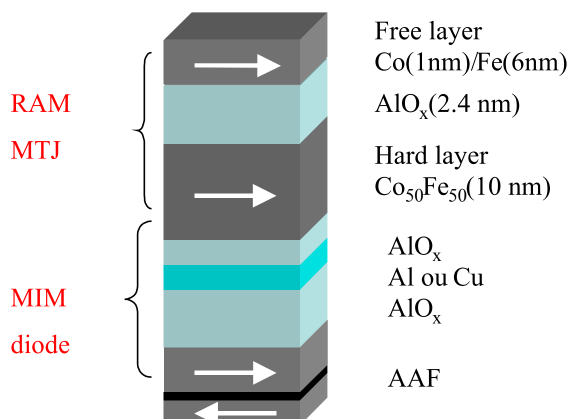


Fig. 9 - MIMRAM stack

When using Cu as metallic intermediate layer in the diode, we obtain a poor asymmetry ratio around 3 (figure 10) with TMR values around 5%. This is not very surprising taking into account the poor reproducibility of the transport characteristics for this system and the small best asymmetry (around 20) ratio obtained for this single diode.

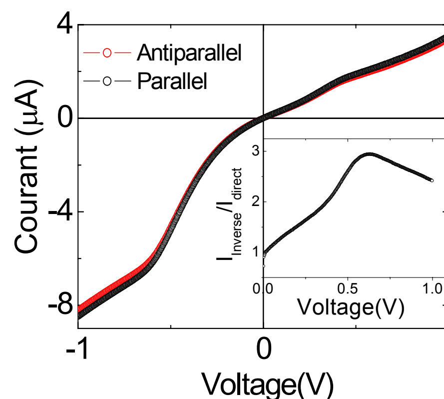


Fig. 10 - I-V curve measured on the MIMRAM stack

With Al as metallic intermediate layer into the diode, we do not get simultaneously a TMR signal and a diode-like behaviour in preliminary measurements. If the junction presents a good asymmetry ratio (figure 11), it does not show any TMR : this lack of TMR is ascribed to similar coercive fields for the "soft" and "hard" layers. On the contrary, when a good TMR signal is measured, the I-V curves are nearly symmetric (figure 12). This is a problem for reading one memory element.

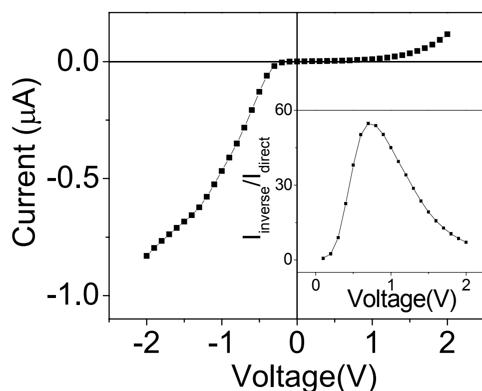


Fig. 11 - I-V curve measured on the MIMRAM stack with Al clusters and without a TMR signal

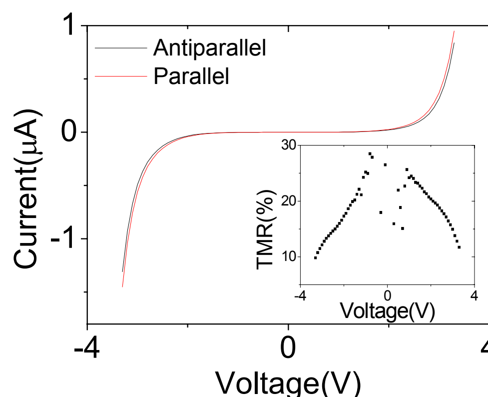


Fig. 12 - I-V curve measured on the MIMRAM stack with Al clusters, with a TMR signal

Then, we decided to vary the conduction properties of the soft magnetic layer in order to recover the expected behaviour of the MIM-RAM. We have explored two directions :

- varying the thickness of the soft magnetic layer : for large thickness, most of the electrons should be thermalized and the conduction through the RAM and through the MIM diode should be a sequential process.
- varying the diffusion in this layer by including a Ru layer : the scattering at the CoFe/Ru interfaces should favour the sequential process.

RAM-MIM system with varying soft magnetic layer thickness

We have grown samples with 5 nm, 20 nm, 50 nm and 100 nm thick soft magnetic layers in addition to the previously grown sample with a thickness of 10 nm. Unfortunately, due to unhomogoneous edging for large metallic thickness, the lithography process in Siemens failed for the two thickest samples. Consequently, we sent the double of these samples to Thales for the 3 terminals process. The result of the measurements for representative junctions on the two thinnest samples are given in the 2 following figures (Fig. 13 and 14). Dissimilar results are obtained for both samples. A large number of junctions exhibit a minimum in the TMR signal around 0 voltage and a few of them exhibit even inverse TMR (negative signal). From the point of view of the MIM-RAM integration, the best junction (Fig. 13-a,b) gives a rectification ratio of 4 at V = 0.8 V where the TMR is around 1 %.

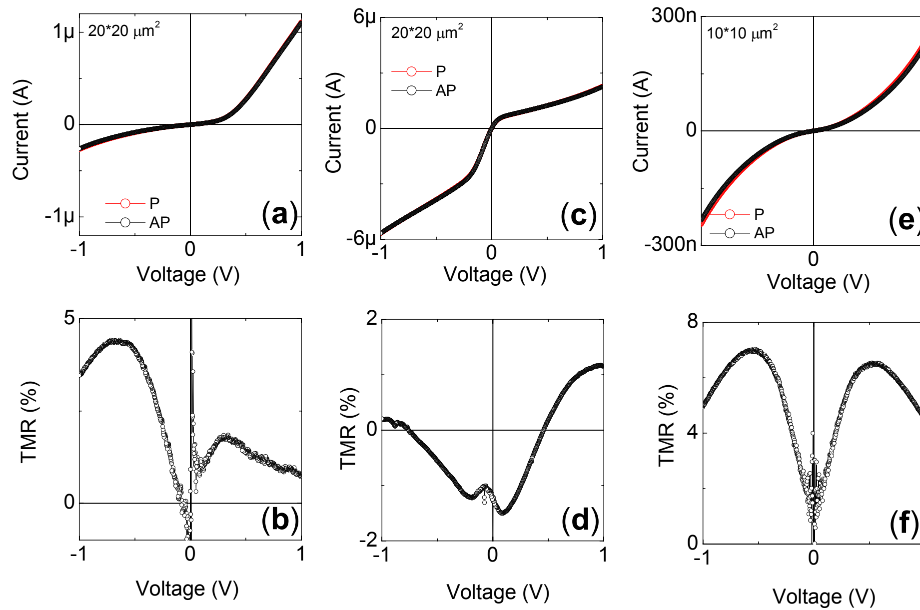


Fig. 13 - I(V) and TMR(V) curves for 3 junctions of the 5 nm thick soft magnetic layer sample. A junction showing a significative rectification and TMR signal (a) and (b), a junction showing an inverse rectification and inverse TMR (c) and (d), and a junction showing no rectification and symmetric TMR with a pronouced minimum around 0 voltage (e) and (f).

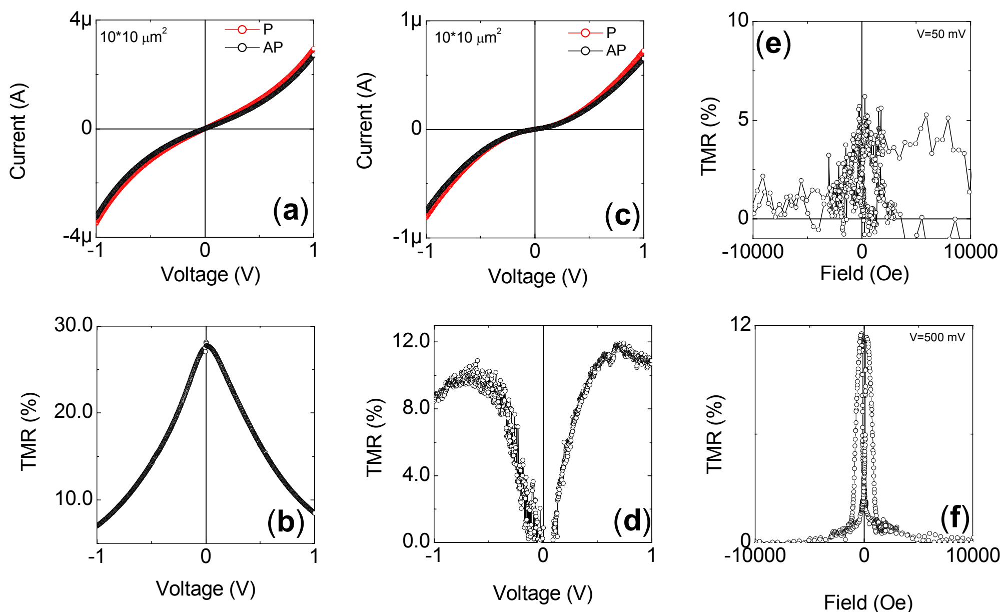


Fig. 14 - I(V), TMR(V) and TMR(H) curves for 2 junctions of the 20 nm thick soft magnetic layer sample. A junction showing no rectification and an usual TMR signal (a) and (b), a junction showing a small rectification and a TMR curve with a minimum around 0 voltage (c) and (d), for this second junction, two TMR(H) curves are given for V = 50 and 500 mV (e) and (f).

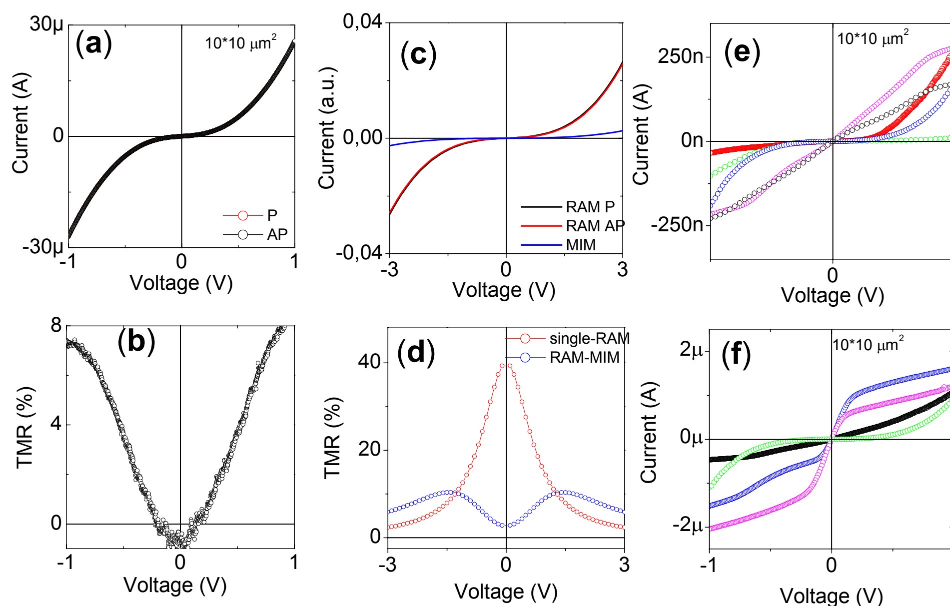


Fig. 15 - I(V), TMR(V) curves for the junction showing a significative TMR signal for Co/Ru/Co as soft magnetic layer sample (a) and (b). The TMR curve with a minimum around 0 voltage could be qualitatively fitted with a simple MIM-RAM model for which the MIM diode has a large resistance (c) and (d). I(V) for a few junctions showing asymmetry or not but no TMR signal (e) and (f).

RAM-MIM system with Co/Ru/Co as soft magnetic layer

For this series, most of the junctions show no TMR signal, a few exhibit a significative rectification and only 2 of them show a symmetric TMR signal (Fig. 15). A simple model of MIM-RAM fits qualitatively the symmetric TMR curves with a minimum around 0 voltage if we assume that the MIM diode has a large resistance as compared to the RAM. This confirms that the resistance optimisation between the MIM and the RAM is the key of success.

Conclusion

Even if the results on a given sample are dissimilar, they are encouraging because :

- some junctions exhibit simultaneously TMR signal and rectification even if they are weak or do not coexist at the same voltage,

- the MIM diode seems to be stabilized as shown by the fact that we changed significantly the underlaying layer (the soft magnetic layer) without loosing the blocking fonctionnality.

These RAM-MIM samples were sent to Thalès in order to process them on a three terminal geometry.

III-1.3.b - TTRAM

At present, only the samples fabricated by UHP exhibit tunnelling in both MTJ after processing, although some degradation of the TMR performance for the bottom junction have been noticed. Nevertheless, these structures were used to perform the first hot electron experiments. In these experiments, a fixed emitter – base voltage V_{eb} is applied, and the collector current I_c is recorded as a function of the base – collector voltage V_{bc}. We present in figure 16 two characteristics measured on a TTRAM structure of the type Glass//Ta/$Co_{80}Fe_{20}$/Co/Al-ox/NiFe/Ta-ox/Co/Ta, for two values of V_{eb}, namely 450 and 625 mV. These experiments have been performed at low temperatures and in a saturating field. The collector current has been normalised with respect to the rectangular bottom junction area.

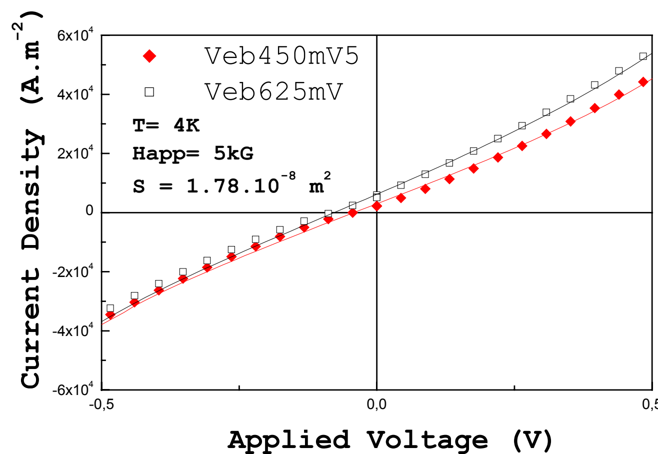


Fig. 16 - Collector current versus V_{bc} recorded for two different values of V_{eb} on a TTRAM structure. Lines are the collector caracteristics computed with the TTRAM free electron model.

The collector current I_c is composed of the direct tunnelling current between base and collector superimposed with the contribution of the ballistic current between the emitter and the collector, occurring mainly in forward bias. A first manifestation of the existence of the ballistic contribution, which is clearly visible in figure 16, is the deviation between the two I-V characteristics observed in forward bias. Unfortunately, we were not able to record the same characteristics at V_{eb}=0 on this sample. Nevertheless, we have tried to extract the ballistic contribution at V_{eb}=0.625 V by subtracting the two curves. This treatment assumes that there is no ballistic contribution at V_{eb}=0.450 V, and is thus an underestimation. The result is plotted in figure 17. From this figure, one can define the asymmetry of the ballistic current as the ratio, for a given voltage, of the forward current to the reverse ballistic current. A second graduation of the ordinates in figure 16 indicates the asymmetry deduced from this treatment. A maximum value of 7 is obtained at 1 V, having in mind that these results are an underestimation due to the lack of measurement at V_{eb}=0.

A second manifestation of the ballistic current contribution lies in the offset of the characteristic (figure 18) and its evolution with V_{eb}. This offset is due to the fact that the ballistic contribution starts to increase in small reverse bias and thus already exists at V_{bc}=0.

We report in figure 18 the evolution of this offset as a function of V_{eb}. The evolution is monotonous and reflects the increase of the ballistic contribution as V_{eb} increases.

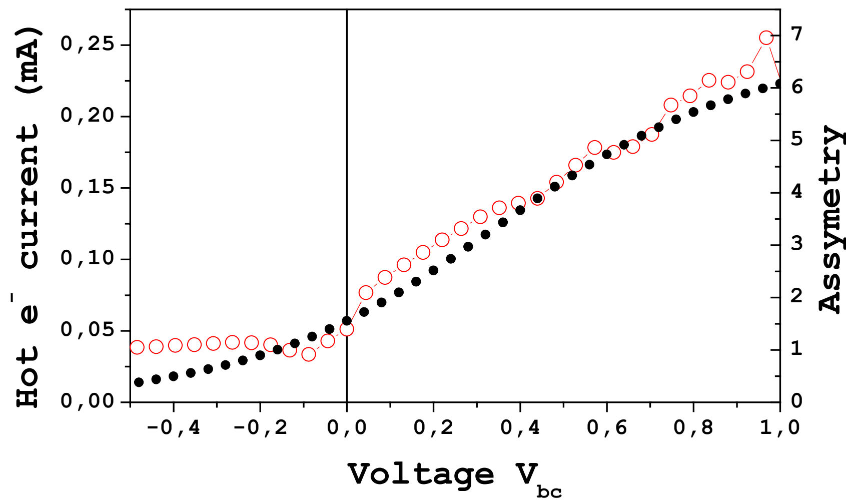


Fig. 17 - Hot electron current and corresponding asymmetry (o) as a function of V_{bc}. The curve (•) is the asymmetry computed with the TTRAM free electron model.

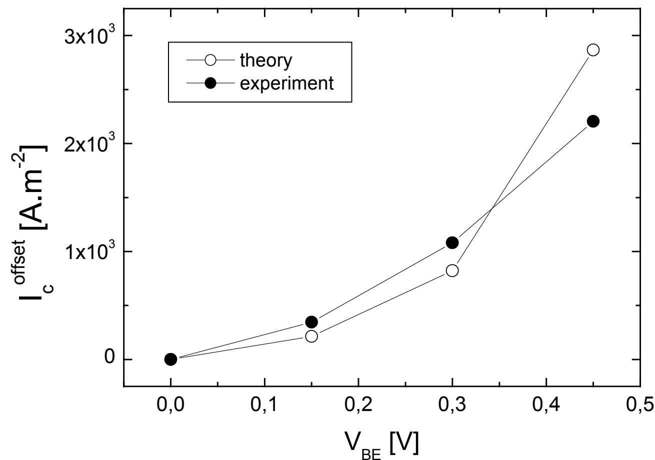


Fig. 18 - Collector current offset as a function of V_{eb}. Comparison between theory and experiments.

In fact the asymmetry can be calculated directly from the total collector current, which corresponds to a dc mode of detection more adequate for a MRAM read protocol than the type of synchronous detection described above. In this frame, the asymmetry is just the ratio of the collector current in forward bias to the one in reverse bias for a given value of V_{bc}, that is :

$$Asymmetry = \frac{I_c(+V_{bc})}{I_c(-V_{bc})}$$

The experimental asymmetry has been derived from this definition based on the results of figure 16. A maximum asymmetry of 40 is observed at V_{bc} = 0.09 V. The existence of this

peak maximum is directly linked with the existence of an offset of the collector current. Indeed, due to this offset, the collector current becomes zero in a slightly reverse bias, which corresponds to the maximum asymmetry.

In the meantime, a model of the electronic transport in TTRAM has been developped, based on the parabolic bands model. This model is described in details in deliverable report D11. We have reported in figure 16 to 18 additional results obtained from this model, based on the use of realistic parameters for the tunnel barriers. The agreement is found to be good in the two cases. More than this, this modelling allows to ascribe the main limitations of present TTRAM performances to the thickness of the filtering tunnel barrier. It predicts that a careful optimisation of this barrier should result in an increase of the asymmetry by more than two orders of magnitude. In addition, the apparent discrepancy between the asymmetries obtained by the two approaches above should be resolved by this optimisation. Indeed, by optimising the thickness of the filtering barrier, we expect the contribution of tunnelling current directly from the base in the collector to become negligible in the range of bias voltage of interest. This should lead to a convergence of the two approaches.

At this stage, one can say that one of the two main objectives associated with the demonstration of TTRAM devices has been achieved, namely the observation of asymmetry as high as 40. This is above the milestone that was fixed in the workplan and the blocking functionality can thus be considered as demonstrated. The comparison between experimental results and modelling allows to validate our model of transport and put in perspective the possibility to increase this asymmetry by more than two orders of magnitude. The second objective, which is the observation of a significant dependence of the collector current with the magnetic configuration between the emitter and the base, has not been achieved at present. This is due to the problems encountered with the TTRAM technology, which we expect to be solved in the coming weeks with the use of the new neutralised ion beam etching source.

The first proof of hot electron transmission has been given at the end of year 2 and major improvements of the current asymmetry characteristics are expected by the use of a source of neutralised ions during multilayer etching. In 36 months, the current asymmetry was then brought from 1 to 40 and an hot electron current has been measured. Furthermore, the comparison between experimental results and modelling allows to validate our model of transport and put in perspective the possibility to increase this asymmetry up to 10^5. Nevertheless, we have shown that etching the top barrier induces defects in the bottom barrier. We expect to solve this problem in the coming weeks with the use of the new neutralised ion beam etching source.

III-1.3.c - Read-write protocol for the memory matrix

A theoretical analysis has been made of the interaction between MIM blocking function and read protocol in practical working Tunnel-MRAM assemblies. The virtual ground configuration has been analysed in conjunction with a ring-of-three closed loop gain element comprising active devices that are currently in widespread use in mobile phone technology. A conflict exists between the stability criteria for this gain element and the read access time. The compromise design parameters used to resolve this conflict are highly dependent on the efficiency of the MIM blocking function incorporated in each Tunnel-MRAM element. Our analysis calculates the optimum design parameters as a function of blocking and predicts sub-nanosecond read access times using state of the art bipolar devices for the gain element.

The 'Virtual Earth' Solution

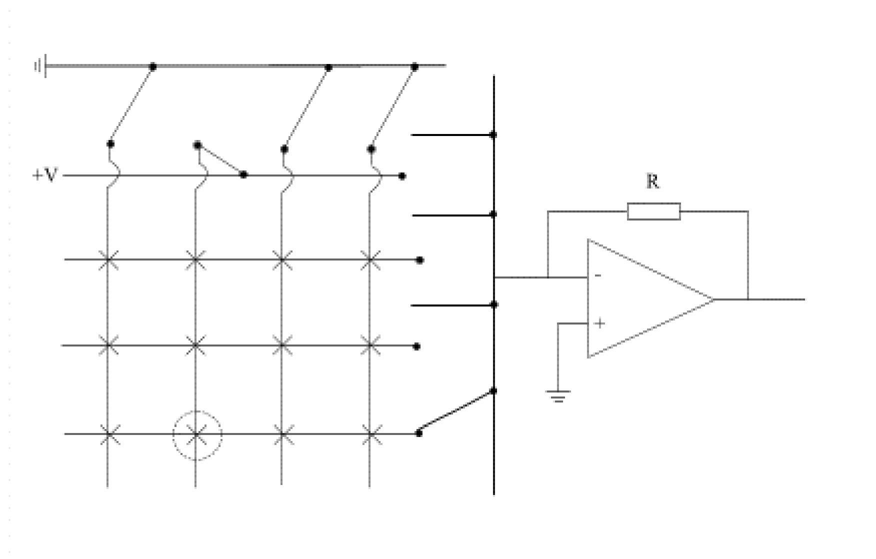


Fig 19: Schematic diagram of the 'Virtual Earth' method or reading an MRAM array.

Consider the lines on which potentials are applied as input lines, and those on which measurements are made as output lines. If all the inputs are connected to Ground, except the one of the cell being measured, which is connected to a positive potential relative to Ground. By connecting one of the output lines to an OP-AMP input, the other input of which is connected to Ground, that output is effectively connected to Ground. This allows the measurement of the current passing through the resistor at the intercept of the two lines.

The ‘Offset Bias’ Solution

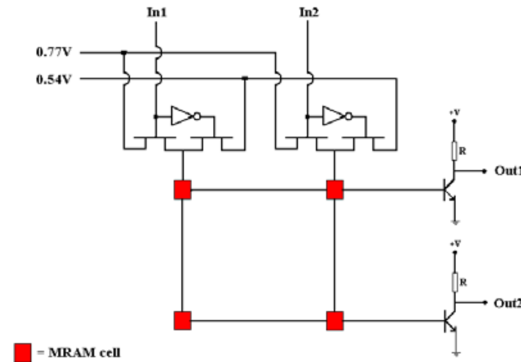


Fig 20: Schematic diagram of the ‘Offset Bias’ method of reading MRAM arrays.

If a transistor is connected to each of the output lines via its base, the emitter of which is connected to ground, then all the output lines will be at approximately the same potential. To measure a single resistance, one of the inputs must have a potential applied to it, and the collector current of the appropriate output transistor measured. The collector current is defined by the current flowing through the resistor of interest. As depicted in Figure 10 the output voltage would be given by;

$$Vo = V - I_c R \,,$$

$$Ic = \beta I_b \,,\; I_b = (V - V_{be}) / R_{cell}$$

A measurement of the output voltage would determine the resistance of the memory cell in question.

This method requires the input lines, other than the one connected to the positive potential, to be left floating or tied to a fixed voltage (the tied wordlines method is shown in Figure 10).

Computer Models were made of arrays connected up in three different configurations. The configurations were:

1. Direct array measurement
2. ‘Offset Bias’ with floating wordlines
3. ‘Offset Bias’ with tied wordlines

The models were based on principles such as the total current flowing onto a floating array line must be zero, and the voltage of a transistor base line has to agree with the current flowing into the V_{be} of the transistor. Each of the models will now be presented in turn.

Model 1 : Direct array measurement

In this model the sum of the currents flowing onto each bitline must come to zero, unless the bitline is the one connected to the cell being measured.

The model was constructed to use an 8x8 array of resistors whose values could be changed. Input parameters to the model were cell resistances for all 64 cells, and the voltage applied to the selected wordline. The model then adjusted the voltage of each bitline until the total current flowing onto each floating wordline was zero. The current flowing on to the selected bitline was then the measurement of the resistance. Other output parameters were the voltages of the floating word and bit lines. The model was used to calculate the resistance measured

when all cells were in the same state and gave a value of $R_{meas} / R_{cell} = 0.234375$. The value when all cells were in the lower resistance state, R, and the measured cell was in the high resistance state, 2R, was $R_{meas} / R_{cell} = 0.265487$. This gave a 'GMR' of 13.27%. This value agrees with that calculated earlier.

A set of 5000 runs was performed, each time randomly varying the cell resistances between two states (R1 = 1.08M and R2 = 2.16M, giving $\alpha = 2$) and calculating the resultant resistance measurement of each of the 64 cells. The data was collected in two columns, one for high active cell resistances, and one for low active cell resistances. The data was then plotted on a graph of current vs frequency of occurrence.

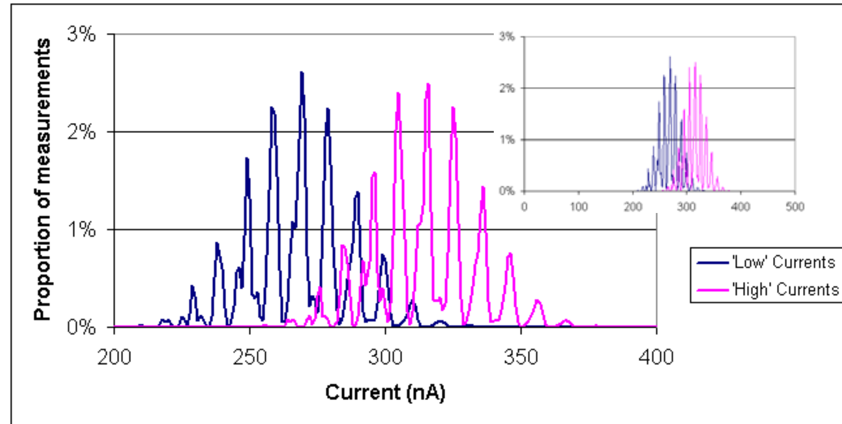


Fig 21: Graph showing the output of 5000 random model runs ($V_+ = 0.1$, $\alpha = 2$).

The region in which the two curves overlap demonstrates the fact that if you measure the resistance of the array using this method you can't necessarily tell which state the cell is in.

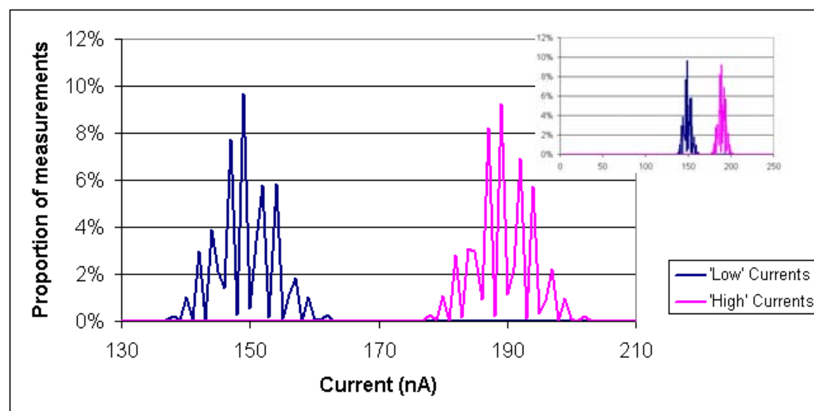


Fig 22 : Graph showing the output of 5000 random model runs ($V_+ = 0.1$, $\alpha = 2$, $\lambda = 0.1$ and $\gamma = 20$).

The model was then adapted to incorporate diode into each of the MRAM cells. The diodes had two parameters (λ and γ) associated with them, which determined the forward and backward resistances:

$R_+ = \lambda R$ and $R_- = \gamma R$

With all resistors in the low resistance state, $\lambda = 0.1$ and $\gamma = 20$ the model calculated a measured resistance of $R_{meas} = 0.443R$ which agrees with the theory presented earlier.

The model was again run with a set of 5000 random array states (with $\alpha = 2$, $\lambda = 0.1$ and $\gamma = 20$) and the data collected, which is presented in Figure 21. Although not happening upon the theoretically lowest GMR of 2.20% the lowest GMR result was 2.98%.

Model 2 : 'Offset Bias' with floating wordlines

In this model the sum of the currents flowing onto each wordline must come to zero, unless the wordline is the one connected to the cell being measured, as well as the current flowing off each bitline into the transistor on that bitline must agree with the V_{be} of the transistor. This model was constructed to use an 8x8 array of resistors. The model adjusted the voltage of each bitline until the total current flowing onto each wordline was equal to zero and the current flowing into the transistor agreed with its base-emitter voltage. The current flowing into each line transistor was recorded as a measure of the cell resistance being measured on that line.

The transistors used in this model were based on the BC184L transistor. I-V curves were measured for 10 BC184L transistors and a function was derived based on the data:

$$I_{cell} = I_b = 3.915 \times 10^{-16}\left(Exp\left[35.8563 \times V_{be}\right] - 1\right)$$

Model 3 : 'Offset Bias' tied wordlines

In this model all the wordlines are tied to specific voltages so it is only the current flowing into each transistor and that transistor's V_{be} that have to agree. Since all the wordlines are tied to voltage levels, each bitline becomes independent of the rest of the array. Two models were constructed, one which modelled the whole of an 8x8 array and one which model a single bitline of 128 cells.

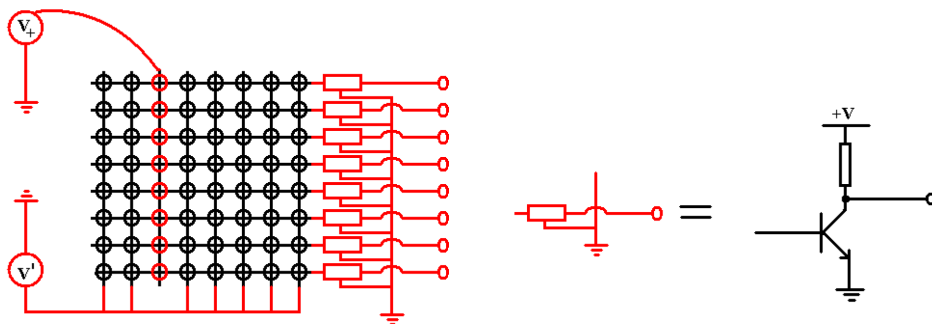


Fig 23: Schematic diagram of an 8x8 MRAM array connected in the 'Offset Bias' Protocol with tied wordlines.

This is the model which was most extensively used since it represents the best method of measuring the array. The effects of changing various parameters were calculated. These parameters were:

1. The cell TMR and resistances.
2. V_+ - the voltage applied to the selected wordline.
3. V' – the voltage applied to the remaining wordlines.

The same transistor model was used as for the 'Offset Bias' with floating wordlines model. The model was later enhanced by the addition of diodes and then finally by the introduction of component errors.

Implication of TMR on array measurements

On initial inspection one might think that increasing the cell TMR would have no drawbacks, but increased TMR also increases the parasitic currents. Refering back to Equation ## we see that the parasitic current is proportional to the difference between V_{be} and the tied voltage V'. Increasing the cell TMR increases the change in current flowing into the transistor in the two different states, and therefore pushes the two V_{be}'s of these states further apart. The difference in V_{be} can be expressed approximately as:

$$\partial V_{be} = V_{be}(R) - V_{be}(\alpha R) \approx \left(\frac{KT}{e}\right) \ln\left(\frac{I_b(R)}{I_b(\alpha R)}\right)$$

$$\partial V_{be} \approx \frac{1}{40} \ln(\alpha)$$

A set of model runs was performed varying TMR values, each run consisting of 250 random array configurations. V_+ was set at 0.8V, giving a cell voltage of approximately 0.25V, and V' was set to 0.544V which is approximately the value of V_{be} for the lower resistance state. The same V' was used for each value of the TMR, though it would be more ideal to use a value closer to the midpoint of the two V_{be}'s given by the two resistance states for each value of the TMR.

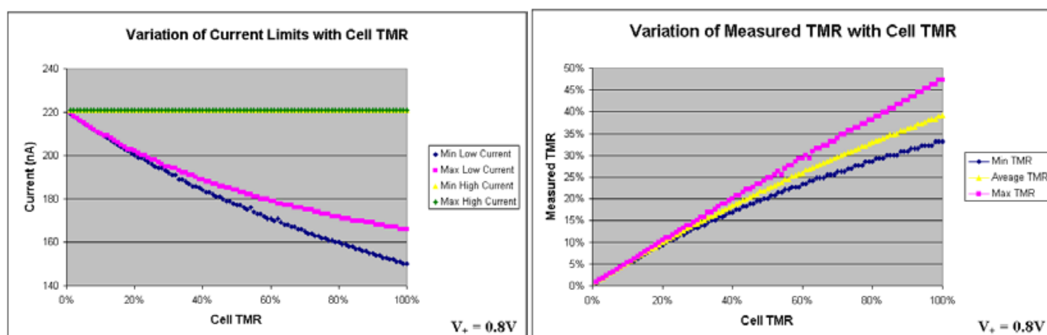


Fig 24: Graphs demonstrating the effect of cell TMR on the measured TMR of an 8x8 array. R=1.08M, α varying from 1 to 2.

The lower limit of the High current region didn't change due to the fact that V' was so close to the V_{be} of that state. The average measured TMR seemed to be approximately half the value of the cell TMR. Increased TMR gives a greater gap between the two ranges of currents measured, but does increase the size of each range.

The larger the value of V_+ the greater the potential difference across the MRAM cells, and consequently the smaller the effect of parasitic currents is. A set of model runs was performed varying V_+, each run consisting of 250 random array configurations. The Cell TMR was set to 100% ($\alpha = 2$, R = 1.08M) and V' was held constant at 0.544V while V_+ varied from 0.6V to 1V. The points at which the Current ranges pinch down are when the transistor V_{be} , for that V_+ and resistance, is closest to V'. The set of runs was then repeated with V' set as the midpoint of the two different V_{be}'s. Th voltage V' is the voltage that the non-active wordlines are tied to, and as such has a direct effect on the parasitic currents. A set of model runs was performed varying V', each run consisting of 250 random array configurations. The cell TMR used was 100% ($\alpha = 2$, R = 1.08M) and V_+ was set to 0.8V.
The final model constructed was a single bitline which consisted of 128 MRAM cells connected in the 'Offset Bias' Protocol with tied wordlines method. Each MRAM cell had diodes and the option to have random MTJ resistance variation. For each model run, a set of resistors was generated that incorporated a variance in the following fashion:

$$R_{MTJ} = \{R, \alpha R\} \times (1 + dR \cdot (1/2 - Random\#))$$

where dR is a defined quantity and Random# is a random number in the interval {0,1}. This model had the option of doing random resistor configurations, or using the four configurations that define the current ranges.

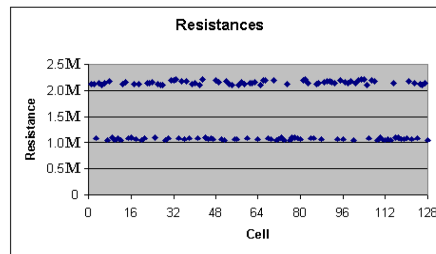


Fig 25: Example variation of cell resistance (dR = 5%)

This model was used to test the effects of variation in Resistance ranging from dR = 1% to dR = 15%, both with and without diodes. When incorporating diodes, it is important that V' be at a lower potential than V_{be}, otherwise the diodes become forward biased, for this reason a value of V' was chosen to be slightly lower than the lowest V_{be}.

The models presented in this section have been shown to agree with the predictions made and have added quantitative answers to the various questions raised in earlier sections. The clear advantages of modelling the arrays in this fashion is the vast number of scenarios that can be calculated and the clear insights it offers into the workings of the various read protocols. The analysis of the various MTJ parameters highlights the importance of not just the TMR value, but also the sustainable cell potentials.

The 'Offset Bias' read protocol with tied wordlines is shown to be the most effective method of array measurement. It has been shown to work with arrays suffering huge resistance variations both with and without diodes. The inclusion of diodes in the MRAM cells does greatly improve the TMR measured, but other considerations may make a bigger difference.

Then, a practical design has been made for read protocol hardware to support the virtual ground wordline Tunnel-MRAM read/address system. The design is based on conventional MOS switching elements as conventionally used in the industry, in conjunction with an ultra-fast ring-of-three closed loop gain element based on state of the art bipolar technology as developed by the mobile phone industry and currently available in surface mount format. This design is capable of addressing multiples of 8*8 TRAM matrices with subnanosecond address time. The address time is independent of the intrinsic timeconstant of the MRAM medium itself.

*III-1.3.c - The 8*8 Array*

An 8x8 dummy array was constructed in order to test the various models and to use as a demonstrator of the different read protocols. Each MRAM cell was represented by two 2.16M resistors and a switch. With the switch in one position the cell had a resistance of 2.16M and in the other position a resistance of 1.08M. These resistances were chosen since they represent a higher challenge for the various read protocols (due to the low currents involved) as well as being a prediction of the resistance of the small MTJ structures that could realistically end up in a production MRAM array.

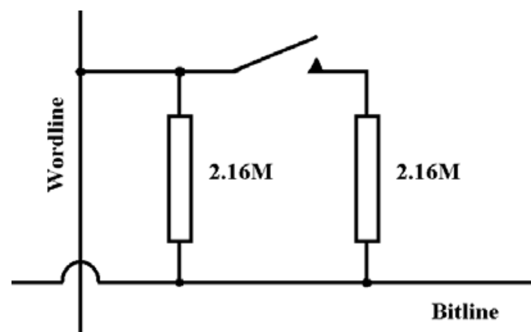


Fig 26 : Circuit Diagram of an 'MRAM' cell model.

First of all the resistance was measured in the four limiting cases and gave resistances (when normalised against the 1.08M low resistance state) . Following these initial measurements the array was connected to a circuit which used the 'Offset Bias' Read protocol.

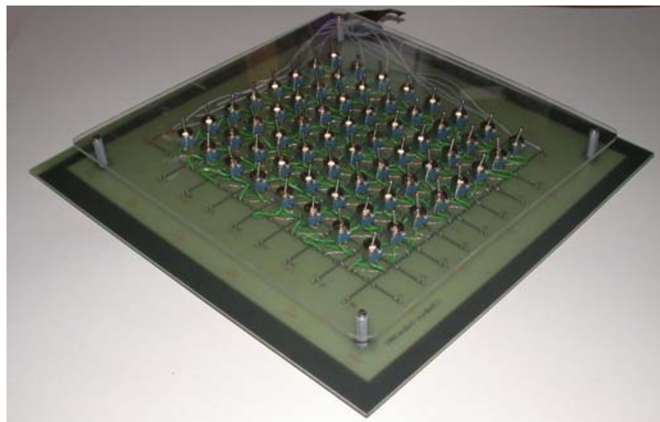


Fig 27: Photograph of the 8x8 macroscopic array of resistors and switches used to model an 8x8 MRAM array.

A circuit board was constructed that consisted of three main parts; wordline drivers, transistor outputs and a power supply unit. The power supply unit consisted of a 78L05 +5V voltage regulator and a couple of operational amplifier circuits. Each operational amplifier was connected to a ten-turn potentiometer so as to give very fine control over its output voltage. Each of the eight wordline drivers consisted of two FET transistors connected to the two different voltage rails (V_+ and V'). If one FET had its Gate voltage raised to 5V it would connect one of the voltage rails to that wordline. The Gate of each FET was connected to a TTL input level (0V or 5V) which was driven by a PC I/O card. The final elements were the transistor outputs each connected to one of the bitlines and having their collector voltages measured by a 12bit 8channel ADC. The 'Offset Bias' Read Protocol was demonstrated to work with an array of resistors, displaying a cell 'TMR' of 100%. An average output TMR of almost 50% was realised with a cell potential of approximately 0.23V and an un-optimised V'. A minimum voltage swing, from high cell resistance to low cell resistance, of 0.585V was observed. Further tuning of output resistors and parameters like V' would give considerably better results.

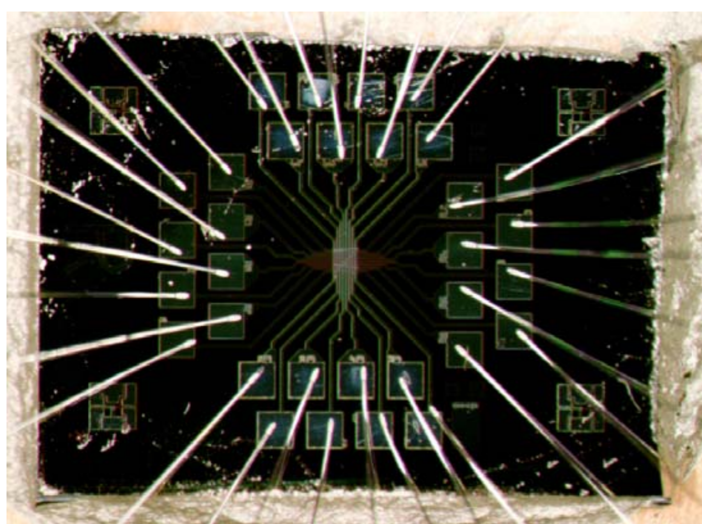


Fig 28 : Photograph of a Siemens 8x8 array wire bonded to the sample holder ready for connection to the 'Offset Bias' Read Protocol circuitry.

Finally, an 8x8 array of MTJs was produced by Siemens AG in Erlangen and connected using the ‘Offset Bias’ Read Protocol (with tied wordlines). The MTJ type used for the array had a TMR in the region of 50% and had very consistent resistances. An array was wire bonded to a special sample holder constructed to interface between the array and the Protocol circuit board.

A large number of cells were damaged in the wire bonding process, but a complete bitline survived. Since each bitline is isolated, there was no effect from the dead cells on other bitlines. The array was manually written to, by changing all the cells from one state to the other, using an external magnetic field (external to the array). Without any optimisation of V’ or the output resistors, TMR values were measured in the region of 10.8-13.2%. Each time a magnetic field was applied to switch the MTJs and then removed the output voltage changed, demonstrating reliable operation. TMRs in the region of 3-4% were reliably read on bitlines with large numbers of dead cell.

The operation of the ‘Offset Bias’ Read Protocol has been demonstrated with a real 8x8 array of MTJ cells, forming a reliable MRAM Matrix.

III-2 Main milestones

The objective of NanoMEM is to develop new families of magnetic random access memories (MRAM) which are based on the spin-dependent tunnelling. In the project program, we proposed first to eliminate the current bottleneck on reducing the size of MRAM cells, i.e. the space taken up by the blocking semi-conducting diode or transistor by implementing MIMRAM (where the blocking is done by a MIM diode of dimensions equal to the memory cell size) or TTRAM (where the spin - transistor itself performs the blocking function). This will allow the length-scale of MRAM cells to be reduced down to 0.1 micron. Then, by the implementation of a matrix of one of the two concept studied in the first phases expected to address the problem of the reduction of the influence of cross-talk for read/write operations when reducing the size cell.

The objectives of the work program appear in which the main milestones of the projects are recalled below

Object	Specification
Junctions	Tunnel junctions with lateral dimensions equal to 0.3 µm
	Tunnel junctions with a barrier with height less than 1 eV and tunnel transport characteristics
	Tunnel junctions with bias field of the detection layer by the hard layer less than 5Oe
	Tunnel junctions with a detection layer which switching field less than 30 Oe
	Tunnel junctions with magneto-resistance of 60 %
TTRAM	Double Junctions composed by 3 magnetic layers with different coercitive field (a difference of 50 Oe between each coercitive field) and 2 barriers of different height (a difference of 0.5 eV between the height of the barriers)
	Technology available for contacting the third electrode on the base of the TTRAM and for the design of the third line of the TT RAM
	TT RAM with blocking functionality with square forward and backward impedances at least lower and at least ten times higher, respectively, than the square tunnel impedance of the storage element
	TT RAM with lateral dimensions equal to 0.3 µm
MIMRAM	MIM RAM with blocking functionality with square forward and backward impedances at least lower and at least ten times higher, respectively, than the square tunnel impedance of the storage element
	Technology available for contacting MIM RAM in arrays of magnetic storage elements
	MIM RAM with lateral dimensions equal to 0.3 µm
Matrix	Matrix of 10 × 10 TT RAMs or MIM RAMs with lateral sizes of smaller than 0.3µm.

At the end of the program, the major part of the specific milestones has been achieved within the consortium. Due to the evolution of the team some aspect have not been studied here. This point have been discussed in the management section. After One year, some important part of researchers and also of materials moved out from the partner ULP which was in charge of the

high frequency part of the work program. Since no one is the consortium have the facilities to produce these experimental jobs, we had to stop the corresponding progress. However, looking to the state of the art progress, we are convinced now that the solution for solving the micromagnetism problems that could occurs at high frequency are already available in the literature. Moreover the concept on which this project is based, the MIMRAM and the TTRAM, do not introduce specific difficulties when looking for the high frequency aspect. So we believe that we can achieve the final device of the project with the actual knowledge based on first generation of MRAM.
Then if we take into account the evolution of the know how in the international community, the totality of our very innovative program have been achieved.

The main results of our work are

1. Tunnel junctions with a barrier height of 0.6 eV and spin dependent tunnel transport characteristics
2. Modelling of single TTRAM cells
3. A TTRAM memory element
4. Simulation of the transport properties of double barrier junctions and first principle determination of the electronic structure of Co/Al_2O_3 multilayers.
5. Elaboration of a MIM diode with a high rectification
6. Electrical model of MIMRAM and TTRAM cells (SPICE) in the array - Estimate of the appropriate diode resistance with respect to information reading
7. Optimised wafer for arrays with excellent magnetic and electric properties
8. Implementation of a read protocol to address system for Tunnel MRAM
9. Practical hardware demonstrator for Tunnel MRAM read access based on the 8*8 TRAM matrix.

III-3 Main deliverables

Deliverable 1 : Project presentation summary
We present here a summary of the 'NanoMEM' project. The overall thrust of this project is to develop two new varieties of Tunnelling-MRAM, MIMRAM (Metal-Insulator-Metal RAM) and TTRAM (Tunnelling Transistor RAM), to the degree where the capability to replace the currently available generation of RAM (which is based on semiconductor technology) in all applications is clearly measurable. In the longer term, the basic science of this project also paves the way for replacing computer hard disks with Tunnelling-MRAM, thus affording much faster memory access times and no moving parts. Compared with other Tunnelling-MRAM architectures, the MIMRAM (two terminal) and TTRAM (three terminal) concepts described offer the advantage of small cell size and hence high packing density, in conjunction with suppression of parasitic signal paths in read and write operations. Commercial prospects of MRAM as compared to alternative non-volatile RAM-systems are then described. The prospects for commercialization are very good in this rapid growing market (15 % yearly) with world wide turnover of 15 billion ECU. The last point of Deliverable 1 gives the main lines of the organisation of the consortium work.

Deliverable 2 : Report on magneto-elasticity modelling for TRAM cells
Reduction of the magnetic bit size to 0.1 microns and below introduces a difficulty in defining accurately the bit shape and induces a relaxation of the strains. Those effects are at the origin of uncontrolled magnetic anisotropies. However, the control of those anisotropies is of primary importance to optimise the magnetic switching in the generation of tunnelling MRAM presently under development. The storage elements contain extremely thin storage layers that are signified by a large interface contribution to the magnetostriction coefficient. The anisotropic strain relaxation due to the structuring of the cells and the word and bit lines results in magnetic anisotropy near the edges of the memory cell which becomes dominant for elements with dimensions less than 0.1 µm. A quantitative model of the magneto elastic anisotropy is therefore needed to forecast the spatial distribution of magnetisation and reversal field due to the anisotropic strain relaxation. This model allows the study of the interface contribution and the nonlinear terms to the magnetoelastic energy.

Deliverable 3 : Report on barrier optimisation
A major actual problem with the reduction of the tunnel barriers lateral size down to 100nm is the fast increase of their electric resistance. Barrier parameter optimisation is then needed in order to get junctions with resistances less than 10 kΩ. For this, two research areas have been developed. In the first one, we continued the study of alumina barriers and we have reduced their thickness down to 8 Å. Then, a major problem with mass production of tunnel junction MRAM is the susceptibility of the tunnel process to small local fluctuations in the insulating barrier thickness. These aspects have been addressed. In the second research area, tunnel barriers made with other materials than alumina have been studied. Especially, insulating barriers of lower barrier height have been studied and magnetoresistance could be measured for barriers made with tantalum oxide. Those low height barriers appear to be good candidates to increase the tunnel current homogeneity.

Deliverable 4 : Periodic Progress Report N°:1 (Covering period 1.1.2000-31.12.2000)

Deliverable 5 : TRAMs with optimised switching characteristics with reversal field less than 30 Oe

Deliverable 6 : Ab initio theory of tunnelling magnetoresistance

The most popular theoretical approach to the problem of tunneling magneto-resistance is based on the Jullière model. However, in this model, the magneto-resistance ratio depends only on the spin-polarized density of states of the ferromagnetic electrodes, and is completely independent of the nature and thickness of the insulating barrier. This conclusion is in striking discrepancy to experimental observations, which show that the nature and thickness of the barrier indeed influence significantly the magnetoresistance ratio. The Jullière model is therefore intrinsically unable to provide a quantitative and reliable theory of this phenomenon. In order to obtain quantitative predictions for realistic systems, it is necessary to rely on *ab initio* calculations. The approach used here to calculate the tunnelling conductance of TMR structures is based upon the Landauer-Büttiker formalism. A particularity of the results is that most of the tunnel current is peaked around a few points of the two-dimensional Brillouin zone, known as “hot spots”. Those regions are quite different for the P and AP configurations. This provides a simple, natural explanation for the fact that the magnetoresistance ratio tends towards 100% with increasing barrier thickness.

Deliverable 7 : First three terminal devices

Deliverable 8 : First MIM RAM with blocking diodes

Deliverable 9 : Mid term evaluation report

We present here our progresses in the investigation of double barriers stacks which theoretically have predicted large current asymmetry ratio, with (TTRAM) or without (MIMRAM) a third contact in the intermediate electrode. With our second generation MIM DIODE, we have observed current asymmetries larger than 25 with good indication that we can still improve it. Although, this contrast (25:1) is still quite small when compared with semiconductor diodes (10^5:1), it represents a very important progress. For comparison, 18 month ago, the best asymmetry experimentally observed was quite small (1.2:1). Simulations of 10x10 junctions matrix have been performed. They give the boundary conditions for having a working device. The actual results are already good enough for the 10*10 matrix, which is the objective of the Nanomem project. Nevertheless, further progress should be made for large matrix compatible to commercial products. Concerning the three terminal device, the material growth bottleneck has been removed since two ‘working’ tunnel junctions with different barrier heights have been stacked. Furthermore, the coercive fields of the magnetic electrodes are different. However, we have observed a net deterioration of the bottom tunnel barrier during the ionic etching of the top tunnel junction. We are now implementing a new procedure, with a neutralisation of the ions, in order to prevent electrostatic breakdown of the lower junction during the ionic etching. Our simulations indicate that a contrast of (10^5:1) is achievable in this TTRAM configuration.

Deliverable 10 : Evaluation of MIMRAM and TTRAM

We present here our progresses in the investigation of double barriers stacks which theoretically have predicted large current asymmetry ratio, with (TTRAM) or without (MIMRAM) a third contact in the intermediate electrode. With our second generation MIM DIODE, we have observed current asymmetries larger than 25 with good indication that we can still improve it. For comparison, 24 month ago, the best asymmetry experimentally observed was quite small (1.2:1). After material growth and technological procedure optimisations, we have observed current asymmetries larger than 20 in our first generation TTRAM cell with good indication that we can still improve it. Indeed, our simulations indicate that a contrast of (10^5:1) is achievable in this TTRAM configuration. Those results is the outcome of 24 months of research during which no current of hot electrons could be measured on TTRAM cells. At month 24, both technologies have reached the same level and both present some difficulties. As far as MIMRAM is concerned, reproducibility has to be improved and work has to proceed on the TTRAM to get the promising 10^5 current asymmetries. Recent use of a neutralisation of the ions during ion etching is one way to prevent electrostatic breakdown of the lower junction. We believe that progresses on both technologies can be met during year 3.

Deliverable 11 : Modelling of two-terminal TRAM cell with blocking diode

We present here our theoretical investigation of double barriers stacks showing that large current asymmetry ratios can be obtained in this samples. With this second generation of MIM DIODE, we show that two transport regimes can lead to high current asymmetries : the hot electrons regime and the resonance assisted regime. We detail these two regimes and present relevant examples of simulated asymmetric I(V) curve and we discuss the role of the key parameters which could be tuned experimentally in order to confirm our predictions and to enhance the asymmetry ratio of 25 obtained experimentally up to now.

Deliverable 12 : Report on cross-talk in arrays of MRAMs

We address, discuss, and predict steps for avoid/reduce the cross-talk between the magnetic elements and/or the control lines of adjacent memory cells is a major problem which is exacerbated by higher packing density requests. The major limitation of the actual devices comes from the high resistivity of the tunnel junction. The simulation showed that an array with this diode has to be operated at high voltage. However this is not intrinsic to the physic of the device, but due to the high thickness chosen in the devices. Identical DIODE with smaller tunnel junctions will lead to lower resistance in the 10 kΩ range will lead as it is shown above to reasonable contrast already acceptable for a 10x10 matrix. We don't see any specific difficulty coming from the implementation of the new concepts : the MIMRAM and the TTRAM. However, this point will be addressed experimentally as soon as 10*10 Matrix will be available. In the last phase of the project, the MIMRAM and TTRAM devices will be optimised with respect to cross-talk

Deliverable 13 : 'Optimised' ferromagnetic electrodes for high spin asymmetry

Deliverable 14 : Periodic Progress Report N°:2 (Covering period 1.1.2001-31.12.2001)

Deliverable 15 : A semi-conductor free diode with a significant increase in the blocking current ratio up to 100

Deliverable 16 : Modelling of the three terminal TRAM cell

A theoretical model has been developed in order to calculate the field dependent transport characteristics of hot electron 3-terminal devices based on magnetic tunnel junction stacks (3TD-MTJ). The three terminal device, which is confronted with technological problems, is predicted to have the highest magneto-current asymmetry. The comparison between experimental results and modelling allows to validate our model of transport. Moreover it put in perspective the possibility to increase this asymmetry up to 10^5. Extensions of the code developed to compute the TTRAM characteristics for non magnetic electrodes and magnetisation reversal of either the emitted, base or collector showed, as expected, that the best configuration consists of a magnetic emitter and base. No significant effect of a magnetic collector has been shown. Nevertheless, a magnetic collector is useful to assert the integrity of the top tunnel junction.

Deliverable 17 : A 'working' single cell (TMR + blocking functionality)

Deliverable 18: Periodic Progress Report : month 36 (Covering period 1.1.2002 31.12.2002)

III-4 Comparison to the original project objectives

As we already discussed in the milestone section, at the end of the program, the major part of the specific milestones has been achieved within the consortium. Moreover, if we take into account the evolution of the know how in the international community, the totality of our very innovative program have been achieved.

After the Catania meeting, we concentrated our work on the proof of both concepts surveyed: the TTRAM and the MIMRAM concepts, followed by the fabrication of the memories matrix. Then the three main objectuives, namely

- ✓ A significant increase in the blocking ratio.
- ✓ A working single cell (TMR + blocking).
- ✓ A TTRAM or MIMRAM matrix.

Have been achieved.

Beside the comparison with the initial objective of the project, we have obtained :

- ✓ A demonstration of the new concept we have introduced in our program, mainly the blocking fonctionality of the new generation of MRAM
- ✓ An Improvement of scientific knowledge with this new nanosystems, multiple tunnel barrier.
- ✓ An Elaboration of know-how to produce these new devices.
- ✓ A large number of high level international publications

III-5 Relations and synergies with other relevant projects

III-6 Benefits for European Society

6.1 Implications for EU policies and standards.

The principal goal of the project was a demonstration of the pertinence of the new concept for the realisation of a second generation of MRAM. Although it is sharply connected with a product with an exponentially increasing market, the success of the project places Europe in good conditions to define the standards in domain of non-volatile memories.

6.2 European competitiveness in a particular market

The success of the project wdid insure a competitive place to Europe in the area of data storage. We should note, that the increase of storage density in Non-volatile RAM will take a part of the market of today's small hard disks for example in portable systems or for intermediate memories, where the **competitive position** of Europe is very bad. Therefore the project is well connected to the European Policy to increase the competitivity of Europe. The radiation hard electronics will also contribute to the European Policy in the domain of

transport with the on-board advance electronics in aeronautics. Since the use of the MIMRAM and TTRAM developed in this project will reduce the failures of the electronics systems the project will also participate to the European policy on the **security** of aeronautic systems.

6.3 Support the future growth of European industry

The success of the project will obviously reinforce the dominant position of the two industrial partners in the area of non-volatile RAM for Siemens and in the area of hard electronics for Thomson-CSF. Moreover, the important increase of storage density we expect with the second generation of MRAM, will take an important part of the market of intermediate size memories for which the only solution is the small size hard disk.
Since Europe is completely outside of the hard disk business, our results will contribute strongly to increase notably the position of Europe in this domain. Other European industries will then take advantage of the results of the project.

The development of ultra low size magnetic tunnel junction devices will also contribute to the field of magnetic sensors. Here the reduction of the size lead directly to a reduction of the price. So the project will increase the European competitivity in this area too. It concerns directly the EC car industry.

The success of the project will obviously reinforce the position of the two industrial partners in the area of application on non-volatile RAM for Siemens and in the area of hard electronics for Thales.

6.4 Protecting and preserving the natural environment and resources;

One of the key advantages of the MRAM concerns the saving of energy consumption. Indeed, the non-volatile character of the data storage in a MRAM device based on magnetic tunnel junctions has the consequence that the device has only to be powered when reading or writing it. In contrast, DRAM devices have to be refreshed many times every seconds and thus, in practice, have to be continuously powered.

The use of magnetic materials instead of semiconductors has no negative impact from the point of view of environment. Indeed, for example in magnetic memories applications, the total volume of new materials to be used in a 1Gbit MRAM device should be less than 10^{-5} cm^3. Moreover the magnetic materials used in the Tunnel Junction structure are neutral for the environment.

The micro and nano fabrication techniques used to define and pattern the magnetic memories are based on dry etching technologies which are consuming less chemical solvents. So the introduction of MRAM will reduce the negative impact on the environment of these aggressive chemical products.

6.5 Quality of life

One of the ultimate objectives of this project is the development of a new generation of non-volatile magnetic random access memories. One of the main impacts of the development of such components is in portable electronics systems. Indeed, the non- volatility, which is

intrinsically associated with magnetism, implies that memories retain the stored information even when the power is turned off. These kind of devices will thus be particularly suitable for use in medical electronics equipment, which, due to their specificity, are extremely sensitive to various kinds of electrical hazards and must thus be hardened. In that respect, this aspect of the project will ultimately have a direct impact on the safety and health of populations.

Moreover, the increase of nonvolatile memory density, will allow to produce hand held electronics or data banks for example in cars.(eg maps etc), where the available space is small and for which at the same time the use of hard disk recording is non applicable

Concerning the application of MRAM to avionics systems, the ultimate impact on the quality of life is straightforward. Indeed, the objective in developing radiation hardened MRAM devices is to improve the reliability of actual memory devices. It will thus directly impact the security of aircraft inboard systems and thus the quality of live of the passengers.

6.6 Employment within the European Union.

At the present level of development in the field of MRAMs, it is clear that Europe is late, in particular with respect to US where companies such as IBM, Honeywell, Motorola. Strengthening the position of Europe, in the perspective of this important technological breakthrough, is also vital in terms of **employment**, which is one of the important policy of the European Commission. The development of ultra low size magnetic tunnel junction devices will also contribute to the field of magnetic sensors. Here the reduction of the size lead directly to a reduction of the price. So the project will increase the European competitivity in this area too. It concerns directly the EC car industry.

IV Future Outlook

During the course of the NANOMEM contract, different companies put a lot of effort on MRAM development. In 2000, Motorola and IBM presented respectively a 0.5 and 1 Kbit MRAM demonstrator. These first protopypes already exhibit write time about 10 ns, making them comparable with SRAM memories.
In 2001, Motorola presented a complete 256 Kbit MRAM using 0.6 µm CMOS technology. This capacity has been extended in 2002 to 1 Mbit. The memory successfully demonstrated by Motorola is a low power (3 V) MRAM based on a memory cell defined by a single transistor and a single Magnetic Tunnel Junction with read and write cycles of less than 50ns. The 64K x 16 memory design is based on a 0.6 micron, 5 metal level CMOS process and was fabricated on a 200 mm substrate using copper interconnects. The cell size is 7.1 µm², the MTJ size being 0.6*1.2 µm². The low power results from an improved reference cell and from flux concentrator (see below). This combination of both innovation allowed to reduce the consumption by a factor 4. Motorola is expected to release a 4 Mbit device using a 0.13 µm CMOS process sometime in 2004. Motorola is associated with Philips and ST Microelectronics to develop a 300 mm manufacturing line at Crolles (France). This unit will manufacture MRAM with a 90 nm process in the following years.

From November 2000, IBM Corp and Infineon Technologies AG are associated in a 50-50 joint venture. Recently Infineon announced an agreement with Altis to tranfer technology to Altis and ramp up a production at this fab. The Corbeil-Essonnes (France) research center of Altis, recently funded by the French government, is specifically designed to industrialize new devices like MRAMs. At the VLSI Symposia in June 2003, IBM and Infineon have presented their high-speed 128 Kbit MRAM core. It is fabricated with a 0.18 µm logic-based process technology. This small base enabled IBM and Infineon to incorporate the smallest MRAM memory-cell size of 1.4 µm² with an access time of 5 ns and a write pulse of 5 ns[1]. IBM and Infineon are working on a proposed 256 Mbit chip they say could be on the market in 2004. IBM is aiming to produce samples that could be issued to device makers by 2004. Potentially, MRAM chips could be mass manufactured by 2005, but IBM will not commit to any plans until demand for these chips begins to appear.

In September 2002, NEC Corporation and Toshiba combined their respective technological capabilities and formed an MRAM development team aimed at accelerating the research and development of MRAM technology and bringing it to the product development level. They announced recently at the 2003 International Solid-State Circuits Conference the successful development of 512 Kbit crosspoint MRAM. Contrary to Motorola and Altis who chose a one transitor per cell architecture, NEC and Toshiba adopted the crosspoint architecture with consists only in a word line and a bit line with a magnetic tunnel junction in between but no transistor. Consequently the magnetic tunnel junctions are not isolated and the signal is diluted by the leakage through the other cells of the array making the signal very difficult to read. To resolve this problem, NEC developed a new cell selection method using a dummy reference cell and a switched-capacitor current sense amplifier that effectively improved the

[1] By comparison, at 90 nm design rules, cutting edge six-transistor SRAM cells are about 1 µm² and DRAM cell sizes are about 0.2 µm² (DRAM cell size is expected to shrink to 0.11 µm² et 65 nm).

signal-to-noise ratio during read operation. The MRAM is fabricated using the company's 0.25 µm CMOS and 0.6 µm MRAM processes.

Cypress Semiconductor Corp. is also very involved in the development of MRAM and formed a subsidiary, Silicon Magnetic Systems, especially devoted to the development of MRAM. Cypress is associated with NVE corporation with a technology exchange agreement. Cypress have recently postponed the release of 64 Kbit and 256 Kbit MRAM initially expected respectively for 2003 and 2004.

Other companies like Samsung, Hitachi, Fujistsu, Honeywell, TSM, USTC and Hewlett-Packard are also working on MRAM. Like all the companies cited above, some of them are seeking agreement and association with others to support the huge efforts necessary to develop and industrialise MRAMs.

As a matter of fact, when new materials are used in semiconductor production, improving yield is always a major hurdle, and manufacturing the TMR element in MRAM is especially difficult. Compared to the semiconductor devices, magnetic tunnel junctions are much more sensitive to any geometrical variation.
The most critical point of a magnetic tunnel junction fabrication is the deposition of the tunnelling insulator. Depositing a 1.2 nm aluminium across a 200 or 300 mm wafer and reproducibly from wafer to wafer is a real challenge. Moreover extremely slight variations in the oxide, on the order of 0.01 nm, can change the magnetic tunnelling junction resistance of MRAM by several percentage points, making the device unpredictable. According to Motorola data, the resistance of a memory cell combining MOSFETs and TMR devices is about 10±5 k .µm². Such a variation of 50% is not acceptable and a self-reference sensing scheme is required[2].
The magnetic properties of the magnetic element are also very dependant on its thickness and its lateral dimensions. New patterning techniques are being developed to ensure reproducible switching properties of the element across the array. Particularly, the IBM-Infineon team used reactive ion etch (RIE) for definition of the magneto-tunnel junction, rather than conventional ion milling (these new development, MRAM specific, requires a strong collaboration with equipment manufacturers[3]). The IBM-Infineon team has been able to control the switching boundary within a 2 percent range across the 128 Kbit array.
The introduction of new materials (particularly ferromagnetic metals) in the manufacturing process is also a problem. Cross-contamination effects are carefully investigated and tests are performed to establish in which extent equipments must be specific or not to MRAM fabrication (considering the cost of any equipment involved in modern semiconductor industry, any specific equipment would increase dramatically the cost of MRAM fabrication).

Current dissipation is also a major problem for MRAMs. In the 128 Kbit IBM-Infineon demonstrator, a 6 mA current is necessary to write a cell. Such high currents involve several problems of consumption, power dissipation, material reliability… And reduction of size of the magnetic element will imply higher switching fields and thus even higher currents. For its 256 Kbit demonstrator, Motorola added a highly permeable, soft ferromagnetic cladding layer to the copper wires, which focuses the magnetic flux generated by the current flowing through the copper wires. This flux concentrator allows to half the writing consumption. Since it also

---

[2] The 256 Kbit Motorola demonstrator includes one reference cell generating a signal midway between the maximum and minimum resistances for 62 memory cell.

[3] From March 2001, Tegal ships a reactive ion etching system dedicated to TMR devices.

focuses the generated magnetic field over the target cell, the cladding layer reduces also crosstalk during writing (a factor which can also limit the density of a MRAM).
For longer range, as for magnetic recording, magneto-thermal writing is also investigated. Magneto-thermal MRAM would use a combination of magnetic fields and ultra-fast heating from electrical current pulses to shrink the stability-limited cell size, reduce the energy required to write data and avoid any crosstalk between cells. Direct writing by spin-polarised current flowing through the junction without any magnetic field would also be an alternative, but this effect is still limited to basic research.

TMR devices are smaller than MOSFETs. In the Motorola 256 kbit demonstrator, the MTJ area is only 10% of the memory cell area. Density can thus be increased by merely shrinking the MOSFET. The crosspoint architecture retained by NEC and Toshiba (which does not include a transistor per cell) suppresses this limit and repels drastically the density limit (this approach is also investigated by IBM-Infineon and Hewlett-Packard). Furthermore, since TMR devices do not necessarily have to be grown on single crystal silicon, several TMR devices can be stacked on each other or on peripheral circuits. According to Infineon estimates, the manufacturing cost for a three-layer chip would be about 15% less than for a flash EEPROM (which has the smallest memory cell area of any semiconductor memory). But the reading problems remain. With the crosspoint architecture, due to the various leakage current, the magnetoresistive signal is drastically reduced and requires improved reading scheme to the prejudice of the access time. Moreover with crosspoint architecture, only one bit can be read at the same time whereas a whole line can be read simultaneously with a MOSFET per memory cell. According to IBM, both approach can be interesting. The one transistor with one magnetic tunnel junction can be optimised for switching speed in embedded applications whereas the zero transistor approach with its higher density is suitable for mass storage applications.
Of course, if the devices proposed in the NANOMEM contract are further improved, the advantages of the high selectivity of the transistor approach and the high density of the crosspoint approach could be combined to achieve a real "universal memory"…

V Information dissemination and exploitation of results

The construction of the consortium web site has been finished in March 2001 (http://www.nanomem.u-nancy.fr). The construction was made around two levels of accessibility. The first one makes the needed publicity of our work on the NanoMEM project and of the projects founded by the EC. In this level, the description of the project is given with a presentation of each partner involved. Links to other EC projects and physics database are also given. A second level with restricted access allows a working space in order to accelerate the information transfer between partners and to share the information of the consortium. This level simplifies the exchange of files needed at time of report writing. In this place, each partner can also find all the files related to the NanoMEM project.

Many of the results have been published in top level international review. We present below the list of the published papers.

List of publications:

1) **Magnetostatic interactions in artificial ferrimagnet based magnetic tunnel junction,** C. Tiusan, T. Dimopoulos, L. Buda, V. da Costa, K. Ounadjela, M. Hehn, H. Van den Berg, accepted for publishing in J. of Appl. Phys (2001)

2) **Spin polarized tunneling as a probe for quantitative analysis of field dependent domain structure in magnetic tunnel junctions,** C. Tiusan, M. Hehn, T. Dimopoulos, K. Ounadjela, accepted for publishing in J. of Appl. Phys (2001)

3) **Local investigation of thin insulating barriers incorporated in tunnel junctions,** T. Dimopoulos, V. da Costa, C. Tiusan, K. Ounadjela, H. Van den Berg, accepted for publishing in J. of Appl. Phys (2001)

4) **Magnetostatic interactions in artificial ferrimagnet based magnetic tunnel junction,** 8th Joint MMM-Intermag Conference, San-Antonio, Texas, January 7-11, 2000.

5) **Spin polarized tunneling as a probe for quantitative analysis of field dependent domain structure in magnetic tunnel junctions,** 8th Joint MMM-Intermag Conference, San-Antonio, Texas, January 7-11, 2000.

6) **Presentation of a keynote lecture entitled "Magnetic nanostructures for spin electronics,** F. Nguyen Van Dau ,Trends on nanotechnology" held in Toledo (Spain), in October 2000.

7) **Nano-materials for the Information Society** , Alain SCHUHL, EC / NSF WORKSHOP ON NANOTECHNOLOGY TOULOUSE, Chamber of Commerce, October 19 and 20, 2000.

8) **Magnetostatic interactions in artificial ferrimagnet based magnetic tunnel junctions.** C. Tiusan, T. Dimopoulos, L. Buda, V. Da Costa, K. Ounadjela, M. Hehn, H. A. M. van den Berg, J. of Appl. Physics 89, 6811 (2001). The 8th Joint MMM-Intermag conference, 7-11 January 2001, San Antonio, Texas, USA.

9) **Spin polarized tunneling as a probe for quantitative analysis of field dependent domain structure in magnetic tunnel junctions.** C. Tiusan, M. Hehn, T. Dimopoulos, K. Ounadjela, J. of

Appl. Physics 89, 6668 (2001). The 8th Joint MMM-Intermag conference, 7-11 January 2001, San Antonio, Texas, USA.

10) **Magneto-resistance and induced domain structure in tunnel junctions.** M. Hehn, O. Lenoble, D. Lacour, A. Schuhl, C. Tiusan, D. Hrabovsky and J.F. Bobo. Mat. Res. Soc. Symp. Proc. Vol. 674, T2.9 (2001). E-MRS Spring Meeting, April 16-20 (2001), San Francisco, Californie

11) **To which extent is the influence of each electrode of a magnetic tunnel junction separable ?** F. Montaigne, M. Hehn and A. Schuhl, accepted for publication in J. of Appl. Physics (2002). The 46th annual conference on magnetism and magnetic materials, Seattle, Washington, 12-16 Novembre 2001.

12) **Tantalum oxide as a low height tunnel barrier for magnetic junctions.** P. Rottländer, M. Hehn, O. Lenoble, A. Schuhl MRS Spring meeting, 16-20 April 2001, San Fransisco (USA).

13) **Domain duplication in magnetic tunnel junctions studied by Kerr microscopy.** O. Lenoble, M. Hehn, D. lacour, A. Schuhl, D. Hrabovsky, J.F. Bobo, B. Diouf, A.R. Fert, Phys. Rev. B 63, 52409 (2001).

14) **Tantalum oxide as an alternative low height tunnel barrier in magnetic junctions.** P. Rottländer, M. Hehn, O. Lenoble, A. Schuhl, Appl. Phys. Lett. 78, 3274 (2001).

15) **Field-dependent domain structure evolution in artificial ferrimagnets analyzed by spin polarized tunnel transport in magnetic tunnel junctions.** C. Tiusan, T. Dimopoulos, K. Ounadjela, M. Hehn, Phys. Rev. B. 64, 104423 (2001)

16) **Domain duplication in ferromagnetic sandwiches.** D. Lacour, M. Hehn, O. Lenoble, A. Schuhl, C. Tiusan and K. Ounadjela, J. of Appl. Phys. 89, 8006 (2001).

17) **Tunnel barrier parameters and magnetoresistance in the parabolic band model.** F. Montaigne, M. Hehn, A. Schuhl, Phys. Rev. B. 64, 144402 (2001)

18) **Determining the interfacial barrier height and its relation to tunnel magnetoresistance.** P. Rottländer, M. Hehn and A. Schuhl, Phys. Rev. B. 65, 054422 (2002)

19) **Hot electron transport in 3-terminal devices based on magnetic tunnel junctions.** D. Lacour, M. Hehn, F. Montaigne, H. Jaffrès, P. Rottländer, F. Nguyen Van Dau, F. Petroff and A. Schuhl. Accepted poster and publication in Intermag Europe 2002 Conference, Amsterdam 28/04-02/05/02.

20) **On the use of exchange biased top electrodes in magnetic tunnel junctions.** D. lacour, O. Durand, J.-L. Maurice, H. Jaffrès, F. Nguyen Van Dau, F. Petroff, P. Etienne, J. Humbert and A. Vaurès, submitted for publication in Appl. Phys. Lett. (2002).

21) **Theoretical study of the relation between interfacial imperfection and transport properties in magnetic tunnel junctions.** D. Stoeffler. Proceedings of MML'01, accepted for publication in JMMM (2002).

22) **Quantum coherent transport versus diode-like effect in semiconductor-free metal/insulator structure.** C. Tiusan, M. Chshiev, A. Iovan, V. da Costa, D. Stoeffler, T. Dimopoulos, K. Ounadjela. Applied Physics Letters 79 (2001), 4231.

23) **Magnetic-roughness-induced magnetostatic interactions in magnetic tunnel junctions**, C. Tiusan, M. Hehn and K. Ounadjela, Eur. Phys. J. B 26, 431 (2002).

24) **Epitaxial MgO layer for low-resistance and coupling-free magnetic tunnel junctions,** E. Popova, J. Faure-Vincent, C. Tiusan, C. Bellouard, H. Fischer, M. Hehn, F. Montaigne, M. Alnot, S. Andrieu, A. Schuhl, E. Snoeck, V. da Costa, Appl. Phys. Lett. 81, 1035 (2002).

25) **Interlayer magnetic coupling interactions of two ferromagnetic layers by spin polarized tunneling,** J. Faure-Vincent, C. Tiusan, C. Bellouard, E. Popova, M. Hehn, F. Montaigne, A. Schuhl, Phys. Rev. Lett. 89, 107206 (2002).

26) **Hot electron transport in 3-terminal devices based on magnetic tunnel junctions**, D. Lacour, M. Hehn, F. Montaigne, H. Jaffrès, P. Rottländer, G. Rodary, F. Nguyen Van Dau, F. Petroff and A. Schuhl, Eur. Phys. Lett. 60, 896 (2002).

27) **The defining length scales of mesomagnetism : a review,** C. L. Dennis, R. P. Borges, L. D. Buda, U. Ebels, J. F. Gregg, M. Hehn, E. Jouguelet, K. Ounadjela, I. Petej, I. L. Prejbeanu, M. J. Thornton, J. Phys. : Condens. Matter 14, R1175-R1262 (2002)

28) **Influence of quantum well states on transport properties of double barrier junctions.** M. Chshiev, D. Stoeffler, A. Vedyayev, K. Ounadjela, J. Magn. Magn. Mater. 240 (2002) 146-148

29) **Magnetic diode effect in double-barrier tunnel junctions.** M. Chshiev, D. Stoeffler, A. Vedyayev, K. Ounadjela, Europhys. Lett., 58 (2002) 257-263

30) **Theoretical study of the relation between interfacial imperfection and transport properties in magnetic tunnel junctions.** D. Stoeffler, J. Magn. Magn. Mater. 240 (2002) 114-116

31) **First-principle investigation of barrier height fluctuations in metal/oxide heterojunctions in relation with large tunnel current fluctuations.** D. Stoeffler, Europhys. Lett., 59 (2002) 742-748

32) **Quantum coherent transport versus diode-like effect in semiconductor-free metal/insulator structure.** C. Tiusan, M. Chshiev, A. Iovan, V. da Costa, D. Stoeffler, T. Dimopoulos, K. Ounadjela, Applied Physics Letters, Vol. 79 (2001) 4231–4233

33) **Hot electron transport in double magnetic tunnel junctions device,** Poster presentation at the International Conference on Magnetism (Rome July 2003) : ,by G. Rodary, D. Lacour, M. Hehn, F. Montaigne, H. Jaffrès, P. Rottländer, F. Nguyen Van Dau, F. Petroff, A. Schuhl

a brief answer with some delay:

1. Sect. III-5
No idea, what is going on in other areas.

2. Sect. III-6

Please write on p. 40, chapt. 4.3:

The success of the project will obviously reinforce the position of the two industrial

partners in the area of application os non-volatile RAM for Siemens and in the area of hard electronics for

Thomson-CSF.

3. Sect. V

References 33, 34 and 35 that refer to work done in Erlangen have nothing to do with the Nanomem project. Please cancel.

I also doubt that in many of the other papers reference has been made explicitly to the Nanomem project which is required by the EC in case this work originated from Nanomem.

4. Other comments: Sect. IV

The Infineon/IBM joint venture from 2000 has nothing to do with Altis. Only recently Infineon announced an agreement with Altis to tranfer technology to Altis and ramp up a production at this fab.

Best regards, Joachim