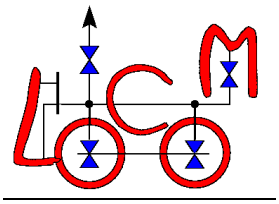
Information Science and Technology

Nanoscale Information Devices



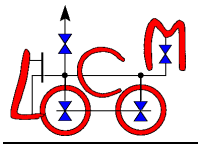
LOCOM

No. 28 844

LOGIC CIRCUITS WITH REDUCED COMPLEXITY BASED ON DEVICES WITH HIGHER FUNCTIONALITY

FINAL REPORT

JULY 1998 - DECEMBER 2000



Content

Introduction

The driving and common idea of all LOCOM members is the development and test of future nanoelectronic circuit designs and architectures. The basic property of exploitation is a negative-differential resistance (NDR) provided by a nano-scale quantum device, namely a resonant or interband tunnelling diode (RTD, ITD). The approach of LOCOM is to test the developed architecture using a presently available high performance III/V based RTD and to proof the transferability to the Si-world using ITDs.

The manufacturabilty of both InP and GaAs III/V based RTDs is demonstrated. It is shown experimentally and by physical simulation that epitaxial growth provides the necessary reproducibility and homogeneity on the atomic scale in order to keep the I-V-fluctuation far below acceptable limits for circuit design. LOCOM has substantially improved the basic building block of the circuits, the monostable-to-bistable logic transition element (MOBILE), towards a very robust, only RTD-area dependent functionality, which rules out non-stochastic errors.

The circuit designs are developed following the threshold logic circuit architectures (cf. ANSWERS project). NAND/NOR operations are experimentally verified. Finally, the work was focussed on the a 1-bit Full Adder as a demonstrator. Though the experimental proof is still pending due to the very complex technology involved, the layout and the SPICE simulation based on experimental device results clearly proof the reduced complexity, the ultra-low voltage operation, and the very high speed. SPICE simulation predict that the LOCOM threshold logic Full Adder is capable of 4 GBit/s which will be the fastest addition circuit, today.

The LOCOM project has hooked-up to the state-of-the-art in tunnelling circuit technology. Intense discussions and co-operations with leading scientists such as G. Klimeck, P. Mazumder, A. Seabaugh, and M. Yamamoto helped us a lot. We are especially indebted to R. Duschl and K. Eberl (Max-Planck-Institut für Festkörperforschung, Stuttgart) for their outstanding SiSiGe layers enabling the experimental proof of the transferability to the Si-substrate.

The LOCOM consortium has presented numerous papers in peer reviewed journals and at international conferences. Finally, we have received many invitations to conferences and special issues of IEEE and Wiles journals on nanoelectronic circuit design and technology.

The transfer to possible commercial applications focused on the availability of a robust, high-speed binary logic module operation with a bias far below 1 V. The possible application in the manufacture of hearing-aid circuits was discussed with the company Siemens (Dr. I. Holube). The establishment of an application nice on a high system level is complicated by the need of several components outside the scope of LOCOM (memory, amplifier, A/D- D/A converters) and highlights the necessity to co-operate with the Si main stream technology. The discussions with Prof. Dr. P. Goetze, Dortmund University, showed that high speed digital filtering for low-voltage mobile applications is an excellent take-up candidate of LOCOM circuits.

The work in LOCOM was exciting and fruitful and thanks to the co-operation of all LOCOM members who made my co-ordinator job focussed on research. I am especially indebted to Christian Pacha and Uwe Auer, who both were the powerful engine of the LOCOM locomotive.

Werner Prost

(LOCOM Co-ordinator)

LOCOM Partners and Members

Partners	Members	Contact
Co-ordination Gerhard-Mercator-University, Center for Semiconductor and Optoelectronics, Solid-State Electronics Dep. Lotharstr. 55, D-47058 Duisburg	**Dr. Werner Prost**	prost@hlt.uni-duisburg.de Tel. +49.203.379.4607, Fax. +49.203.379.3400,
Gerhard-Mercator-University Center for Semiconductor and Optoelectronics, Solid-State Electronics Dep. Lotharstr. 55, D-47058 Duisburg	Prof. F.-J. Tegude, Dr. Uwe Auer, Dipl.-Phys. J. Degenhardt, Dr. Werner Prost	tegude@hlt.uni-duisburg.de Tel. +49.203 379 3391, Fax +49.203 379 3400
University of Dortmund Lehrstuhl Bauelemente der Elektrotechnik, Emil Figge Str. 68, D-44221 Dortmund	Prof. Karl Goser, Dr. Christian Pacha, Dipl. Ing. Peter Glösekötter	goser@luzi.e-technik.uni-dortmund.de, Tel +49 231-755 2021, Fax -755 4450
TU Eindhoven Faculty of Electrical Engineering, Postbus 513 NL-5600 MB Eindhoven	Dr. Theo van de Roer, Dipl. Ing. Guido Janßen	T.G.v.d.roer@ele.tue.nl Tel +31 40-247 5106, Fax -244 8375
Forschungszentrum Jülich GmbH Institut für Schicht und Ionentechnik, Postfach 1913, D-52425 Jülich	Dr. Arno Förster, Dipl. Phys. Jörg Malindretos, Dipl. Phys. J. Stock	a.foerster@fz-juelich.de Tel. +49 2461-61 2361, Fax - 61 2333
University of Surrey School of Electronic Engineering UK-GU2 5XH Guildford	Prof. Mike J. Kelly, Dr. R. K. Hayden	M.Kelly@ee.surrey.ac.uk Tel. +44 1483-259 410, Fax +44 1483- 534 139
IST Project Officer European Commission, Dir. General Information Society, Technology, Information Society Technology, Rue de la Loi 200, B-1049 Brussels	Dr. Ramón Compañó	Ramon.Compano@cec.eu.int Tel.: ++32-(0)-22.959.580, Fax.: ++32-(0)-22.968.390 Office: Av. Beaulieu 33 3-22, B-1160 Brussels

web-page LOCOM Project:

http--www.hlt.uni-duisburg.de-research-d_research_main.asp

Project Overview

Technical Summary

The subject of this proposal is *the design and fabrication of small-scale circuits of linear threshold gates with multiple terminals* consisting of resonant tunnelling diodes (RTD) and heterostructure field effect transistors (HFET). This combination allows the realisation of linear threshold networks as a novel logic scheme for parallel computation beyond Boolean logic. The objective is a qualitative performance increase of circuits for arithmetic functions due to reduced circuit complexity and finally increased computational functionality. The goal of using novel circuit architectures composed of modular building blocks is to solve some serious problems of future nanoelectronics such as the increased interconnection density, the complexity of the design and the demand for parallel operation on the gate level. Due the availability, a carefully commissioned III-V-based technology will be used for the realisation of demonstrator circuits.

Project Workplan, Deliverables

The work to be done in LOCOM and its strong relationship with the ANSWERS project is depicted in Figure 1. In addition, the flow of information within LOCOM and from/to ANSWERS can easily be seen. The circuit simulation will be carried-out in the ANSWERS project. Device parameters for RTD and HFET will be provided as input data of circuit simulation of demonstrators. The III/V technology is following a physical device simulation and a carefully assessment with respect to manufacturability. The realisation of demonstrators is based on this advanced technology.

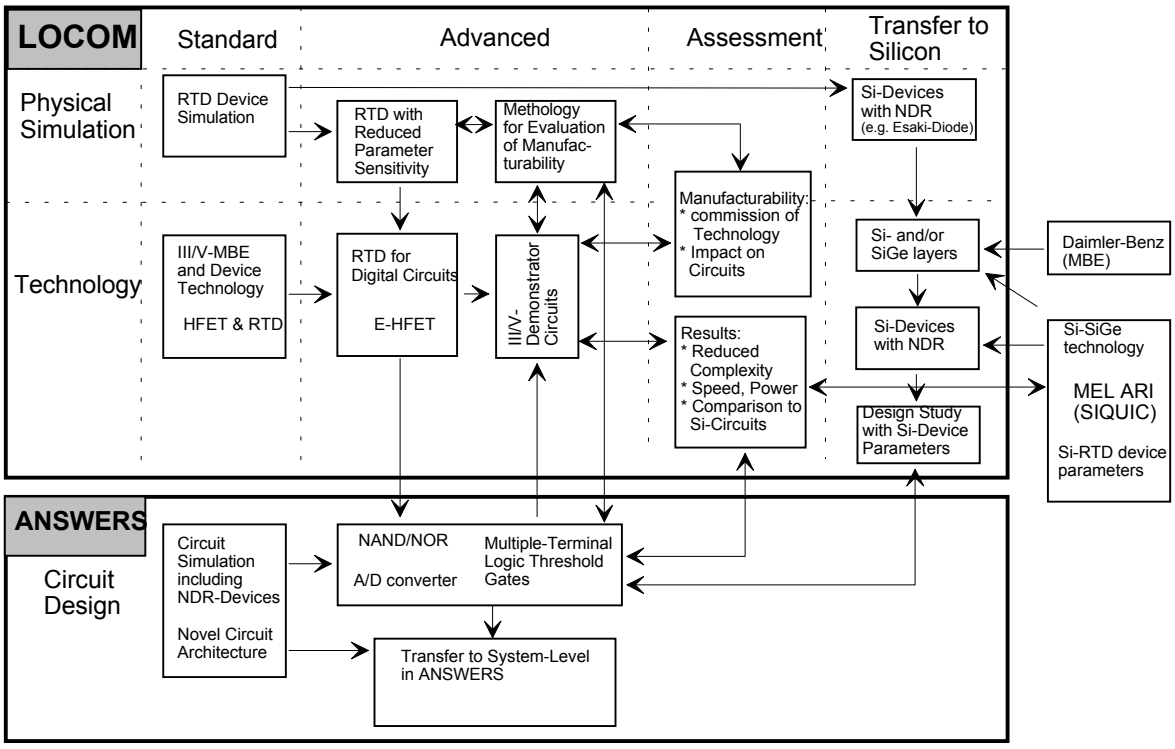


Figure 1: LOCOM project overview and the relationship to ANSWERS

Structure of the work

The project comprises four workpackages. Each workpackage will be organised by one of the partners who has the main responsibility in that area. The different tasks of the workpackages and their relationship and a list of milestones and deliverables are displayed in tables 1-4 and fig. 6. The work package responsibilities and the assignment of the tasks for each partner are:

Table 1: Technical Workpackages

	WP 1 ANSWERS WP2	**WP 2**	**WP 3**	**WP 4**	**WP 5**
	UNIDO Goser	**GMUD Tegude/Prost**	**TUE v.d.Roer**	**GMUD Prost**	**LOCOM Partners**
	Circuit Design and Architecture	**Technology (III/V-based)**	**Device Simulation**	**Evaluation of Manufacturability**	**Transfer to Si**
.1	NAND/NOR Gate	Evaluation of material in the sub-nm scale	Parameter sensitivity in physical simulation	Device level tolerance	Design and experim. study on Si-Based NDR Devices (TUE, UNIDO, SiQUIC, Daimler Benz)
.2	Multiple terminal LTGs and full adder	Fabrication InP-based RTD/HFET	Layer structures with low parameter sensitivity	Circuit level tolerance	Internal MEL-ARI exchange with Si-technology (SiQUIC)
.3	Functional tests and Fan in/ Fan out studies	Experimental study on manufacturability	Si NDR Devices (Simulation)	Planar RTD technology	
.4	Transfer to system level and reverse engineering	Demonstrator: (i) NAND/NOR, (ii) multiple term. threshold gates, (iii) full adder		Industrial manufacturability analysis	

Table 2: Time Schedule of workpackages and Tasks

No	WP Name	WP No	Partner	Man Month	Year 1				Year 2				Year 3	
					3	6	9	12	15	18	21	24	27	30
1	**Circuit Design and Architecture**	**1**	UNIDO / ANSWERS	**33**										
2	**Technology (III-V based)**	**2**	**GMUD**	**36**										
2.1	Evaluation of material	2.1	GMUD	3										
2.2	Fabrication InP-based RTD/HFET	2.2	GMUD	9										
2.3	Experimental study on manufacturability	2.3	GMUD	6										
2.4	Demonstrator Circuits	2.4	GMUD	18										
3	**Device Simulation**	**3**	**TUE**	**24**										
3.1	Parameter sensitivity in phys. simulation	3.1	TUE	9										
3.2	Layer structures with low par, sensitivity	3.2	TUE	9										
3.3	Si-NDR Devices	3.3	TUE	6										
4	Evaluation of Manufacturability	**4**	**USG**	**24**										
4.1	Device level tolerance	4.1	TUE	3										
4.2	Circuit level tolerance	4.2	UNIDO	3										
4.3	Planar RTD technology	4.3	GMUD/FZJ	-	◆	◆		◆	◆		◆	◆	◆	
4.4	Industrial manufacturability analysis	4.4	GMUD/ USG	6			◆			◆				◆
5	Transfer to Silicon	**5**	**UNIDO**	**6**										
5.1	Exper. study of Si-NDR dev.	5.2	UNIDO	*[1]										
5.2	Exchange with Si-technology	5.3	All/ external		◆				◆			◆		
6	**Project Management**	**6**	**All**											
6.1	Project Coordination	6.1	GMUD	8										
6.2	Coordinative Meetings	6.3	All		◆		◆		◆		◆			◆
6.3	Web page	6.4	UNIDO		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆
6.4	Status Report	6.5	All					◆				◆		
6.5	Final Report	6.6	All											◆
7	**Take Up of Results**	**7**	**All**											
7.1	Knowledge Exchange: Technology	7.1	GMUD				◆					◆		
7.2	Si-industry and Si-research	7.2	All						◆			◆		
7.3	Transfer to system level	7.3	UNIDO		◆					◆				

Table 3: Milestones

No	Month	WP	Partner	Milestones
1	3	2.1	GMUD	Evaluation of material properties for device fabrication
2	6	2.2	GMUD	Fabrication and test: RTD/HFET combination
3	9	2.2	GMUD	Parameter Extraction for SPICE simulation models
4	9	2.4	GMUD/ANSWERS	Fabrication and test: NAND/NOR gate with modifiable threshold
5	15	2.4	GMUD/ANSWERS	Fabrication and test: three terminal LTGs (Weights: 1,2,4, Thresholds 1...7)
6	24	2.4	GMUD/ANSWERS	Fabrication and test: Depth 2 Full-adder circuit
7	9	3.1	TUE	Model for InP-based RTDs operative
8	18	3.2	TUE	Assessment of InP-based RTD parameter sensitivities
9	24	3.3	TUE	Model for Si-based NDR device operative
10	18	4.1	TUE	RTD device tolerances
11	27	4.2	UNIDO	LTG circuit tolerances
12	24	4.3	GMUD/FZJ	Tolerances of planar technology
13	30	4.4	GMUD/USG	Industrial manufacturability study completed
14	29	5.1	UNIDO, TUE	Equivalent circuit model and device structure for Si-based LTGs
15	29	5.2	All, SiQUIC	Strategy for Si-Transfer

Table 4: Deliverables

No	Month	WP	Partner	Deliverables
1	6	2.2	GMUD	Device Parameters for SPICE simulation models delivered to UNIDO
2	12	2.4 3.1	GMUD/ TUE	Experimental Results of NAND/NOR logic family Simulation of InP-based RTD I-V-Characteristics
3	18	2.1 4.1	GMUD, TUE	Delivery of material parameters for study of manufacturability Report on first tolerance study on RTD devices delivered to partners
4	24	3.2 2.4, 4.4	TUE GMUD	RTD structure design for minimum sensitivity, Experimental Results of LTG circuits, Report on Progress on closing the reverse engineering loop
5	30	5.1, 3 4.2, 5 4.3, 4.4	TUE UNIDO GMUD / FZJ / USG	Si-based NDR device models and designs, Report on Device Simulation, Circuit level tolerance, Circuit Designs for Si-based LTGs, Report on Si-Transfer Planar technology tolerances, Industrial manufacturing analysis,
6	33	6	GMUD	Final Report

Form 5.1: Schedule of deliverables

Project N°: 28 844 Acronym: LOCOM

Types of deliverables	No. Table 4	Description of the deliverable (Title)	Availability C - R - P (1)	Workpackage reference	Responsible/ involved partner	Project month
YEAR 1	1	Device Parameters for SPICE simulation models delivered to UNIDO	R	2.2	GMUD	6
	2	Simulation of InP-based RTD, Experimental Results of NAND/NOR logic family	R	3.1 2.4	TUE GMUD	12
YEAR 2	3	Delivery of material parameters for study of manufacturability Report on first tolerance study on RTD circuits delivered to partners	R	2.1, 2.3 4.1	GMUD TUE	18
	4	RTD structure design for minimum sensitivity First Experimental Results of LTG circuits, Report on Progress on closing the reverse engineering loop	R	3.2 2.4 4.4	TUE GMUD	24
YEAR 3	5	Si-based NDR device models and structure designs, Final Report on Device Simulation Circuit Designs for Si-based LTGs Report on Si-Transfer Final report on industrial manufacturability	P	5.1 3 5.1 5 4.3, 4.4	TUE TUE UNIDO UNIDO GMUD	30
	6	Final Report	P	5	GMUD	33

(1) Availability: C = confidential, R = restricted, P = public

WP 1: Circuit Design and Architecture

The workpackage WP1 has been carried out in the ANSWERS project (no 28 667, WP 2) in close co-operation with LOCOM. The workpackage is described in the ANSWERS report in detail. Resonant tunnelling device circuits using the MOBILE principle [Maezawa 93, Chen 96] have been the starting point of this work.

Device simulation

The basic device configuration for digital logic circuit applications is a monolithically integrated Resonant Tunnelling Diode-Heterostructure Field Effect Transistor (RTD-HFET), where the RTD is placed in the drain contact layer of the HFET. To simulate and design these circuits UNIDO has developed several large signal equivalent circuit models for RTDs and HFETs. The equivalent circuit models have been incorporated into HSPICE which is a commercial version of the Berkeley SPICE circuit simulator. For HFET modelling the built-in MESFET model has been adjusted.

In addition, a simplified 3-terminal Resonant Tunnelling Transistor (RTT) model has been developed. This speed up simulations of larger circuits. Characteristic feature of this model is the extension of the RTD equivalent circuit by a gate-voltage dependent pre-factor that varies between 0 and 1. The pre-factor reduces the HFET to a switching function and enables a greater flexibility to use other three terminal resonant tunnelling devices such as gated RTDs, where a transistor function is obtained by a Schottky wrap around gate.

Concerning the RTD-HFET concept the DC parameters have been extracted from the I-V characteristics in co-operation with LOCOM, GMUD, for, RTDs with different peak voltages and peak currents and HFETs with 1.0 µm gate length.

Resonant tunnelling device system development

Device parameter specification

The compatibility of the logic input and output voltage levels is of basic relevance for the proposed logic gates and requires a careful selection of the RTD peak voltage V_P. For InP-based RTD-HFETs the logic high voltage level is limited by the forward conduction of the HFET Schottky gate to 0.7-0.8 V. Since the logic voltage swing of the RTD-HFET logic gates is a function of the I-V characteristics ($\Delta V \approx 1.5\text{-}2.5\ V_P$) RTDs with a low peak voltage of $V_P = 0.3$ V have been selected.

To estimate the delay and the transition times of the logic gates the RTD-speed index, that is the ratio of the RTD peak current I_P and the total load capacitance, has been introduced. By varying the RTD peak current density j_P and together with the nominal geometrical capacitances of RTD and HFET (C_{RTD} = 6-7 fF/µm^2 and C_{GS} = 4.8 F/µm^2) the speed index can be adapted to the special requirements of the logic gates. Since GMUD is capable of fabricating RTDs with peak current densities between 5-100 kA/cm^2 this allows a great flexibility in the sense of a speed power trade-off.

A technological problem with a significant impact on the circuit design is the fabrication of enhancement-type InP-based HFETs with threshold voltages larger than 0.1 V. Since the logic voltage levels of RTD-HFET gates are V_L=0.05 V and V_H = 0.7 V a threshold voltage of V_{T0} = 0.3 V would be the optimal solution to maximise the noise margins. This observation is somewhat surprising because at the beginning of the project it was expected that the RTD

fabrication is more critical than the HFET which is the more conventional device from the viewpoint of exploiting quantum effects in logic circuits. Thus, the first demonstrator circuits are fabricated with depletion type HFETs (V_{T0} = -0.09 V).

NAND/NOR gate

The elementary circuit configuration for RTD-HFET logic gates is the Monostable-Bistable Logic Transition Element (MOBILE). The MOBILE is composed of two RTDs with pulsed power supply acting as a rising edge triggered latch. In the original version the logic input stage is made of HFETs connected parallel to the RTDs. To optimise this circuit configuration and to meet the requirements of a "good logic family" following modifications are introduced:

a) The first improvement is the substitution of the input HFET by a monolithically integrated RTD-HFET combination (cf. technical report). The I-V-characteristics of such an RTD-HFET exhibits a NDR-like behaviour for a HFET channel current higher than the RTD peak current IP. The RTDs in the input branches are limiting the total current under open channel conditions. In this case the precision requirements of the HFET parameters are relaxed to a switching function ($I_D << I_P$ or ID >> I_P) while in the conventional case the HFET has to provide an exactly defined amount of current at a distinct bias voltage.

b) To avoid the pulsed power supply of the original MOBILE the load RTD has been replaced by a further RTD-HFET combination, where the HFET gate serves as an input for the clock. This enables the use of a constant supply voltage $V_{DD} \approx 0.9$ V and separate clock buffers (inverter chains) to generate the phase overlapping clock signals. A further improvement is achieved by inserting a pull down HFET in the output branch. This pull down HFET, controlled by an inverse clock, speeds up the discharging of the load capacitance and significantly reduces the delay time of the high-low transition. Since MOBILE gates require a multiphase clocking scheme this inverse clock signal is available and will not cause an additional circuit overhead.

c) In a third step, a more stringent approach is made where the driver RTD of the MOBILE is simply omitted. A comparable output behaviour is kept but the total current is drastically lowered due to the smaller load RTD area. Hence the average switching power consumption is reduced from 0.94 mW to 0.3 mW at the cost of a smaller fan-out.

As first demonstrator an inverting Boolean logic family containing two-terminal NAND and NOR gates as well as a programmable NAND/NOR gate has been designed and fabricated. The characteristic feature of the programmable NAND/NOR gate is a third terminal which is used to modify the logic function. The HFET gate length is 1 µm, the width 10 µm; the input RTD area is 3 µm^2. The threshold voltage is V_{TH} = -0.09 V and the peak current density is j_P = 9 kA/cm^2.

Functional tests and fan-in/fan-out studies

Functional tests have been performed for a 2-input NAND/NOR gate proving the functionality for the critical logic input combinations of (1,0) = (0,1) by switching one input RTD-HFET from low to high. Although depletion type HFETs were used the compatibility of input and output logic voltage levels has been demonstrated. In addition, the amplification during the monostable-bistable transition has been verified by reducing the input voltage swing below 100 mV. Based on these results HSPICE simulations for different load capacitances and scaled devices (200 nm gate length, 1 µm^2 RTD areas) indicate a maximum fan-out of at least 4. The rise time of the clock signal is 10 ps and the clock period is below 200 ps so that GHz operation should be possible with sub-µm scaled devices.

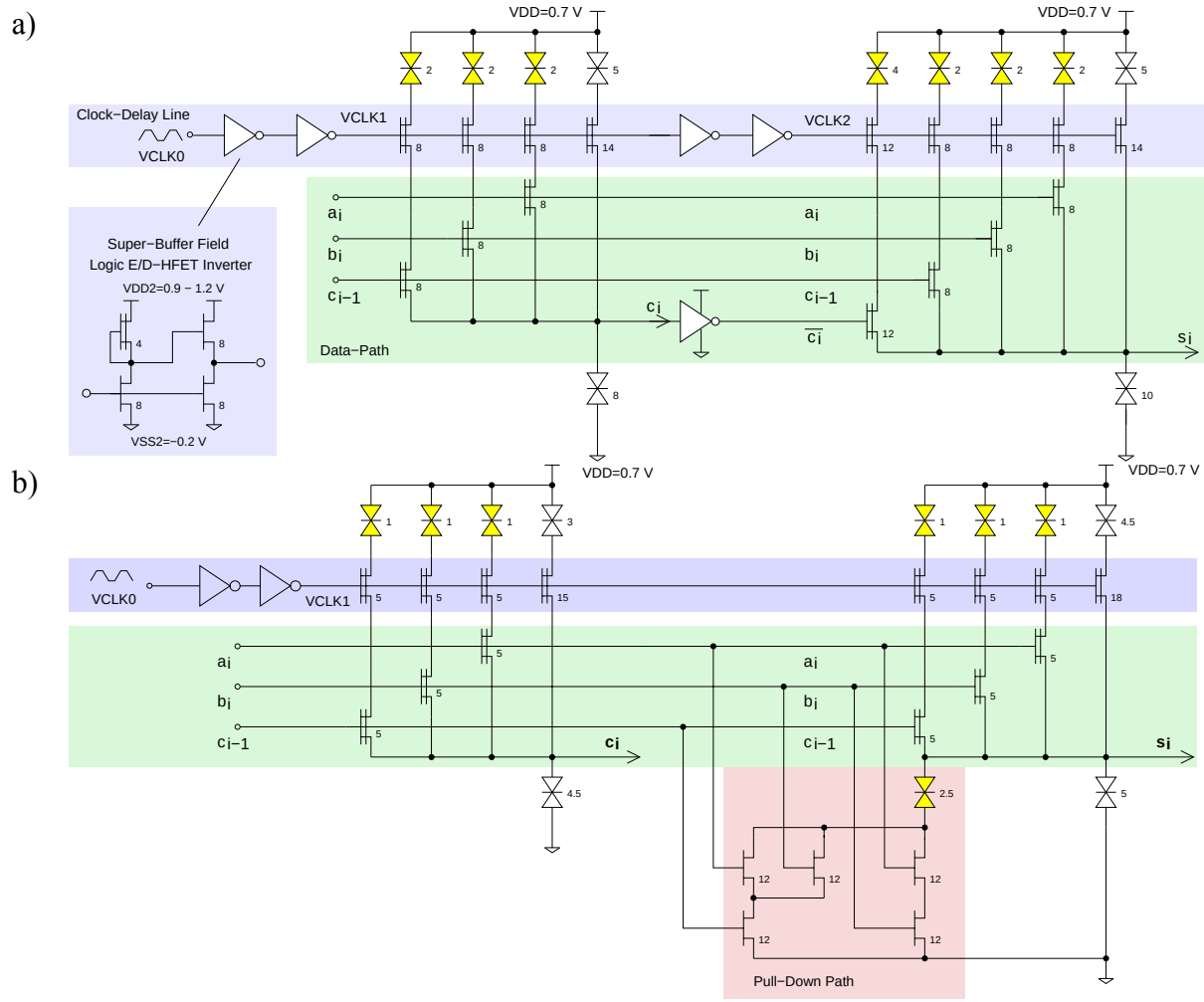


Fig. 1.1 : Two-stage Threshold logic full adder (a) with local clock generation by an E/D HFET SBFL inverter chain and one-stage hybrid full adder (b) with Boolean pull-down path for a fast sum computation.

Design of a full adder demonstrator circuit

The demonstrator circuits for the RTD-HFET threshold logic MOBILE gates is a depth-2 full adder. At the end of year 1 different alternatives were under discussion. Among these, two alternative approaches are selected for fabrication by the LOCOM project. Both designs are made of two logic gates which is the minimum number of gates to implement an full adder (Fig. 1.1). The supply voltage is V_{DD}=0.7 V and the clocking frequency obtained from SPICE simulation is f_{CLK}=1 GHz.

The first full adder consists of two linear threshold gates in a two-stage circuit arrangement (Fig. 1.1a), whereas the second design is a hybrid approach between Boolean logic and threshold logic (Fig. 1.1b). In both circuits one gate is required to compute the carry bit c_i and a second gate to compute the output sum s_i. Since the carry propagation chain is the critical path gate in an n-bit ripple carry adder composed of serially interconnected full adders, the designs are optimised in regard to a fast carry computation.

The advantage of the hybrid approach is a simultaneous computation of the carry and sum in the same logic stage so that this design is ideally suited for a high bandwidth bit-level pipelined multiplier. The simultaneous computation is achieved by embedding a Boolean logic pull-down

path in the sum gate. In contrast to the threshold logic version the inputs of this pull down path are connected to the original operands a_i, b_i and c_{i-1} and thus the sum computation is independent of the carry computation. Therefore, both gates in Fig. 1.1b are controlled by the same clock signal V_{CLK0} and can be tested separately.

The pure threshold logic adder has been chosen to test the driving capability and the propagation of logic signals in a multi-stage circuit with bit-level pipelining. For on-chip clock generation an inverter chain composed of SBFL-E/D HFET's is used (inset in Fig. 1.1a). The rising edge of the clock signal V_{CLK2} has a phase shift compared to V_{CLK1} of two inverter delays. This ensures that the evaluation of the inputs stage of the sum gate s_i (Fig. 1.1a) only starts if the output of the preceding stage, that is the carry c_i is valid. The layout of the adders has been made by GMUD for 1 μm^2 and 2 μm^2 RTD areas.

Functional tests and fan-in/fan-out study

The fan-in/fan-out study has been made for 2-input MOBILE AND and NAND gates implemented with RTD-HFET input stage and conventional HFET-only inputs devices as proposed in the original MOBILE by the group at NTT. Moreover, the peak current density was increased to j_P=80 kA/cm^2. The output rise and delay time increases linearly with the load capacitances (Fig. 1.2). The time scale of several ps underlines the attractiveness of MOBILE logic for multi-GHz operation. The results obtained by transient SPICE simulation are shown in Fig. 1.2. Due to the signal input in the pull-up device and the larger gate overdrive due to the depletion type input devices the non-inverting AND gates are slightly faster than the inverting NAND gates.

Since the full adder circuits have not been fabricated yet the functional test are not started. However, a test pattern scheme has been developed so that all input combinations of a full adder

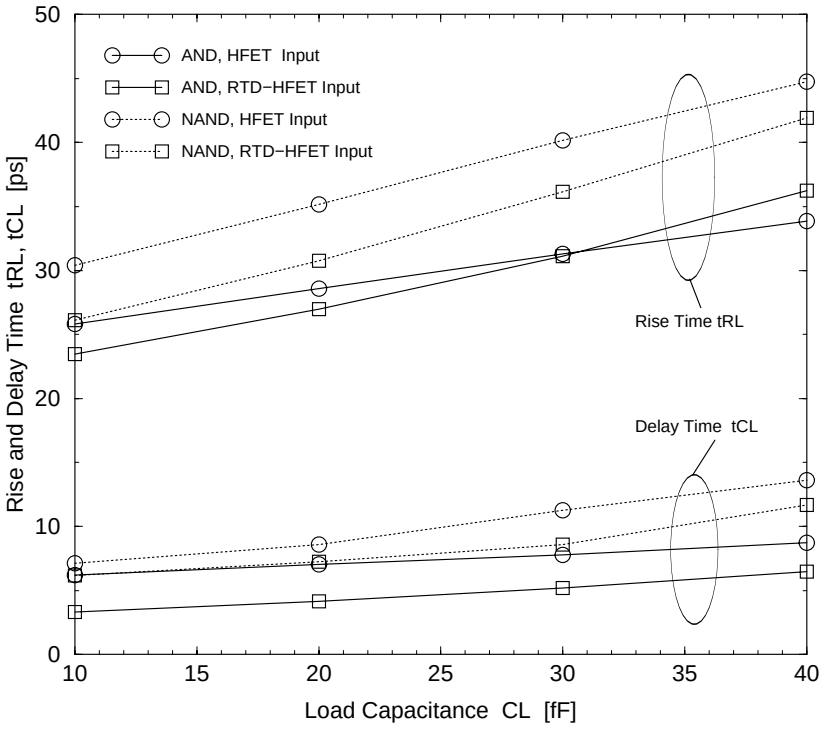


Fig. 1.2: Fan-out study of 2-Input (FI2) MOBILE logic gates with HFET (Boolean) and RTD-HFET (threshold logic) input stage. A FO of one (FO1) corresponds to a load capacitance of CL=10 fF for 200nm HFET gate length.

(0,0,0), (0,0,1), (0,1,1), and (1,1,1) can be tested as a alternating output sequence of 0101-0101 for the carry and 0000 1111 pulses for the sum. To generate these output patterns a measurement system composed of a high speed pulse generator (up to 3 GHz) for the clock signal and the input operands (a_i, b_i)) and an HP 81010A bit-pattern generator for the incoming carry c_{i-1} (0000-1111 sequence) is built by UNIDO and GMUD. The logic inputs (a_i, b_i) are switched every second clock cycle and the incoming carry c_{i-1} is changed every 4-clock cycles due to the frequency limitations of the programmable bit-pattern generator of f=125 MHz. It is intended to operate the full adder circuits for a high speed test at f_{CLK}=1.2 GHz clocking frequency and for functional tests at f_{CLK}=100 MHz. Since it is difficult to modify the fan-out for this first set of test circuits, based on the experimental results the fan-out study will be performed by SPICE simulation.

WP 2: Technology (III-V based)

This workpackage aims at the fabrication of novel monolithically integrated resonant tunnelling diodes (RTD) and heterostructure field-effect transistors (HFET) for logic circuits with reduced complexity based on the monostable-bistable transition logic element (MOBILE) concept. The impact of material properties and the manufacturability of quantum devices have to be investigated and the functionality of the novel approach has to be demonstrated.

Task 2.1 Evaluation of material in the sub-nm scale

The impact of material properties on the device and finally circuit characteristics has to be evaluated using final devices. Conventional test structures for photoluminescence are suited to evaluate the principal properties. For final layer structures a novel X-ray method has been developed which allows a direct determination of strained InP-based RTDs.

Task 2.2. Fabrication of InP-based RTD and enhancement-type HFETs

The InP-based heterostructure field-effect transistor (HFET) has been developed in the GMUD group since 1990 for analogue applications and since one year also for digital applications. The main task here is the development of an enhancement-type HFET which is presently in several groups under investigation. The gate-metallisation and the undoped InAlAs Schottky barrier layer will be optimised for a large barrier height to guarantee the compatibility of input and output levels.

Task 2.3 Experimental study on manufacturability

For the study on manufacturability measurements of material and device parameters are carried out. Additionally growth and technology parameters will be delivered to evaluate critical parameters of the circuit fabrication. First material parameters will be extracted in WP2.1. First results will be considered in the fabrication of RTD/HFET combinations in WP 2.2, from which a further evaluation of critical parameters will be performed.

Task 2.4 Demonstrator Circuits: NAND/NOR gates and multiple terminal LTGs

The circuits developed in WP 1.1 and WP 1.2 will be monolithically integrated on InP-substrate based on the design rules evaluated from WP 2.3. First NAND/NOR gates will be fabricated to show the bi-stable characteristic of the RTD circuit, followed by three terminal LTGs with reduced circuit complexity. The completion of the experiments will be a depth-2 full adder, which demonstrates the enhanced functionality of the LTG-circuits and which will prove the performance of the enhancement-type HFET. The experimental results are to demonstrate the manufacturability of logic gates with reduced circuit complexity and enhanced functionality due to the use of devices with NDR. The demonstrator circuits will be the precursors for Si-based circuits with reduced complexity.

Introduction

The **mo**nostable-**bi**stable transition **l**ogic **e**lement (MOBILE) for logic circuits consists of two series connected RTDs which are monolithically integrated with parallel HFET input branches [Maezawa et al. 1993]. A substantial improvement of the original MOBILE circuit is the substitution of the input HFET by a monolithically integrated RTD/HFET combination (= **r**esonant **t**unnelling **t**ransistor: RTT) (cf. Fig.2.1, right). The I-V-characteristic of such a RTT exhibits a NDR-like behaviour for a HFET channel current higher than the RTD peak current I_{peak}. The RTDs in the input branches are limiting the total current under open channel conditions. In this case the precision requirement of the HFET parameters is relaxed to a switching function ($I_D << I_{peak}$ or $I_D >> I_{peak}$) while in the conventional case the HFET has to provide an exactly defined amount of current at a distinct bias voltage.

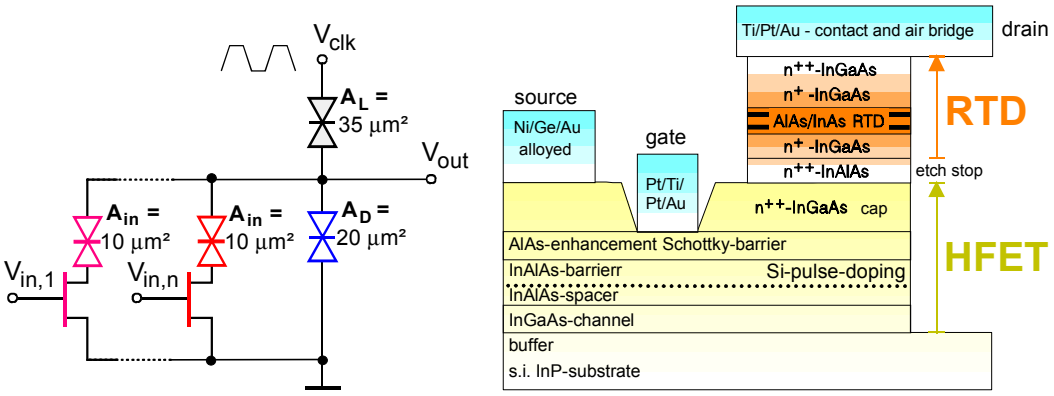


Fig. 2.1: Layout of the novel NAND/NOR MOBILE (left) using RTT input stages (right).

Because the switching functionality of these novel MOBILE's only depends on the RTD area ratio, the reproducibility and homogeneity variations in terms of lithography, etching or epitaxial growth are substantially cancelled. Moreover, for the input logic combination (1 0) and (0 1) the steady-state power consumption is drastically reduced.

WP 2.1 Evaluation of material in the sub-nm scale

A non-destructive analysis of strained centre symmetric double-barrier resonant tunnelling diodes layers is developed. In the measured (004) rocking curves the intrinsic barrier-well-barrier sequence results in a beat under the strained layer peak which can be used for layer analysis down to the nine monolayer range. Based on the kinematical theory analytical relations are deduced which allow a direct correlation of the measured rocking curve data to barrier and well thickness and composition. This method is applied to InP-based double-barrier resonant tunnelling diodes and is proven to be applicable to final devices including thick but lattice matched contact layers.

In fig. 2.2a the measured (400) reflection curves of a highly strained InGaAs/InAlAs DB-RTD test structure are shown. The compressively strained high In-content well results in a layer peak on the low angle side of the substrate. On the high angle side a beat is clearly detected. Using the analytical relations (Haase et al. 1998) the intrinsic DB-RTD layer parameters can be calculated. The lattice matched $In_{0.53}Ga_{0.47}As$ contact layer thickness of about 100 nm can not be deduced from the kinematical model. A contact layer thickness of 102 nm derived from the high frequency Pendellösung and the analytical data are taken as input data for the dynamical theory simulation given in fig. 2.2b. An excellent agreement between measured and simulated in rocking curves is obtained without a time consuming trial and error procedure despite a

substantial deviation from the nominal layer data. In fig. 2.2c a rocking curve without thick contact layers is simulated clearly showing that the above described features of the rocking curve are not affected. The main difference is the high frequency Pendellösung superimposed in fig. 2.2a,b due to the thicker contact layers. This comparison proves that the analytical description of the intrinsic DB-RTD structures holds also in the presence of thick contact layers. This way it is possible to characterise final DB-RTD device layer sequences.

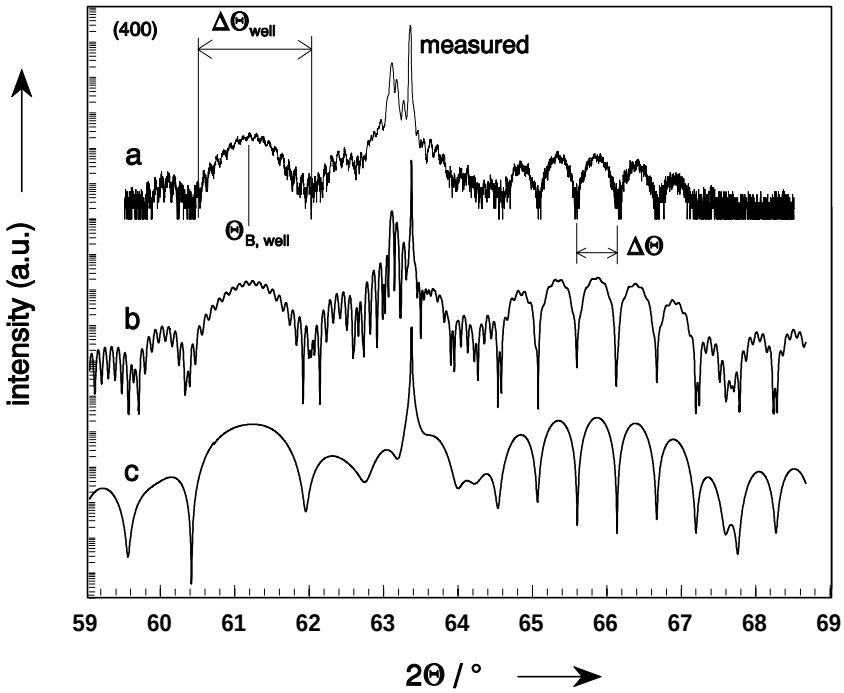


Fig. 2.2. (004) x-ray diffraction rocking curves of an InGaAs/InAlAs DB-RTD: (a) measured and (b-c) dynamical simulations using data from analytical relations applied to the measured curve. Curve (c) is simulated without contact layers.

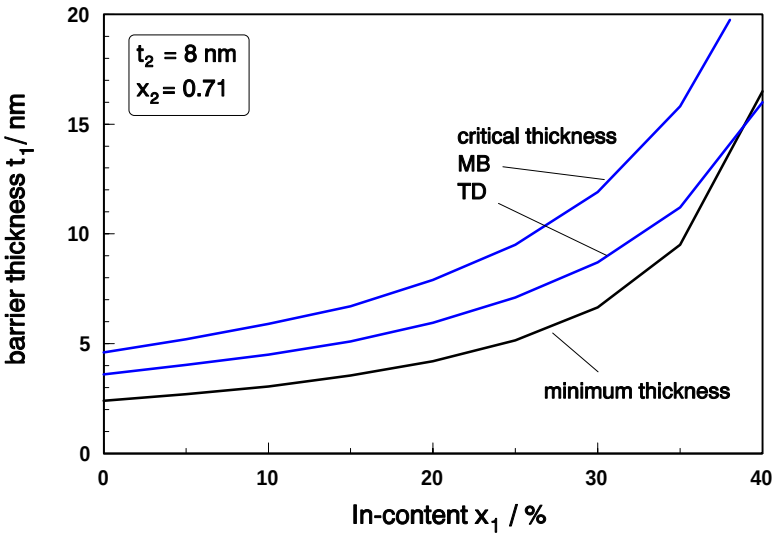


Fig. 2.3 The minimum thickness of the barrier layer as a function of In-content for a full separation of the intrinsic DB-RTD beat from the substrate peak in comparison to the maximum allowed (critical) thickness after Tsao and Dodson (TD) and Matthews and Blakeslee (MB).

In fig. 2.3 the minimum thickness for a full occurrence of the beat from the intrinsic DB-RTD is compared with the maximum allowed thickness from a critical thickness analysis taken from the literature [Tsao and Dodson 1988, Matthews and Blakeslee 1974]. The well layer is fixed here to t_2 = 8 nm $In_{0.71}Ga_{0.29}As$ (x_2 = 0.71) and the contact layers to 100 nm lattice matched $In_{0.53}Ga_{0.47}As$.In fig. 2.3 curve TD (Tsao and Dodson]) and MB (Matthews and Blakeslee) give the critical layer thickness of the DB-RTD barrier layers based on the force balance model according to the single (TD) and double (MB) kink mechanism, respectively. This is an important criterion because it is well known that strain relaxation by appearance of misfit dislocations leads to a breakdown of the Pendellösung fringes. Fig. 2.3 shows that in the whole interesting Indium-content range a whole set of data for the analytical description of the intrinsic DB-RTD can be provided. On the other hand the required strain is high and quite close to the limits deduced from the critical thickness analysis. But a wide variety of DB-RTDs is just designed close to this limit in order to take full advantage of the available material properties. In case of high current density devices very thin barrier layers are required and a full separation of the beat from the substrate may not be provided. Nevertheless in most cases the beat frequency is still detectable and gives easily the sum of barrier and well thickness and the mean lattice mismatch, respectively.

The deduced analytical data allow a direct evaluation of the intrinsic DB-RTD layer sequence even in the presence of thick contact layers and in a wide range of strain and thickness. A DB-RTD layer design close to the critical thickness criterion favours a full analytical analysis while even in case of very thin layers (≤ 9 monolayers) a precise description of the sum of barrier and well thickness is available.

WP 2.2 Fabrication of InP-based RTD and enhancement-type HFETs

The InP-based layer stacks were grown by solid-source molecular beam epitaxy (MBE) on exact (100) oriented s.i. InP:Fe-substrate (cf. Fig. 2.4, left). The undoped intrinsic highly strained RTD structure is grown at T_g = 420 °C. It consists of two 2.2 nm undoped AlAs barriers and the In(Ga)As well. The well is composed of 8 monolayer (ML) InAs symmetrically sandwiched between 4 ML lattice matched InGaAs-smoothing layers. The intrinsic RTD is sandwiched between highly doped contact layers grown at 520 °C which facilitate a non-alloyed ohmic contact. A doped 10 nm InAlAs-etch-stop layer is inserted assisting the lateral under etching of the self-aligned metallisation between anode and anode pad. The device fabrication starts with the evaporation of a non-alloyed RTD-anode finger electrode (30 nm Ti / 30 nm Pt / 340 nm Au). Next, the RTD-layer stack is etched down to the InAlAs-etch-stop layer. In a second etch step the cathode mesa is defined while the RTD-anode finger is under-etched in order to isolate the anode pad. Finally, the RTD-cathode metallisation is evaporated (30 nm Ti / 30 nm Pt / 100 nm Au) building a self-aligned and non-alloyed ohmic contact.

The DC I-V-characteristic of the RTD with an emitter area of 6 µm² is given in Fig. 2.4, right. The RTD-current linearly increases to its peak of about 5 kA/cm² at a peak-voltage of about 0.23 V. The peak-to-valley ratio is about 3 which is high enough for digital applications.

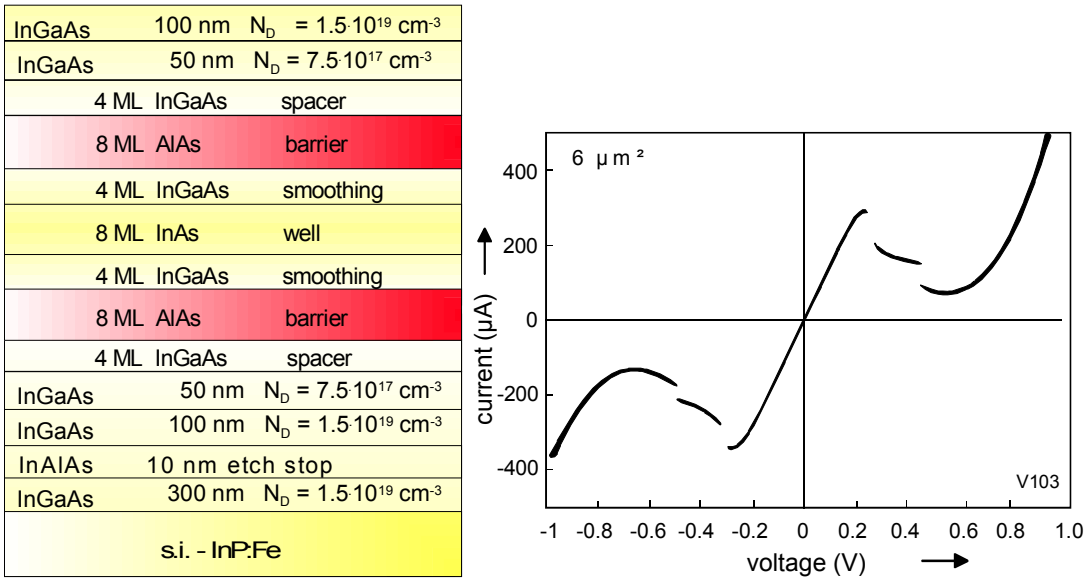


Fig. 2.4: Layer structure (left) and I-V-characteristics of an InP-based RTD (right)

Table 2.1: InP-based E-HFET layer sequence (ML: monolayer = 0.3 nm)

Layer	doping	thickness
InGaAs-cap	$6 \cdot 10^{18} cm^{-3}$	5 nm
InGaAs		5 nm
InAlAs		10 nm
AlAs		8 ML
InAlAs		5 nm
δ-doping	$2 \cdot 10^{12} cm^{-2}$	
InAlAs		8 ML
InGaAs-channel		20 nm
InAlAs-buffer		70 nm
substrate s.i. InP:Fe (001)		450 µm

Technology of enhancement type HFET

In order to switch a logic gate, the output voltage of the driving gate has to be lower than the threshold for the off-state or below the maximum allowed bias voltage for the on-state. In this case, the utilisation of an enhancement-type HFET (E-HFET) is advantageous since the gates based on depletion-type HFETs are relatively complex to fulfil the above requirement. E-HFETs in the InP material system are a critical issue because of the low Schottky barriers available. The layer structure of an E-HFET for digital applications is given in Table 1. In the InAlAs Schottky barrier layer 8 ML AlAs are inserted and the sheet doping density is reduced to $2 \cdot 10^{12}$ cm^{-2}. The corresponding I-V-characteristics are depicted in Figure 2.5. The threshold is +0.1 V and the transistor is operable up to a gate bias of +1 V. The E-HFETs with a gate length of 1 µm exhibit a transconductance of 240 mS/mm. For the intended maximum gate bias of 0.6 V, the gate leakage is below 2 mA/mm and hence suitable for logic circuitry.

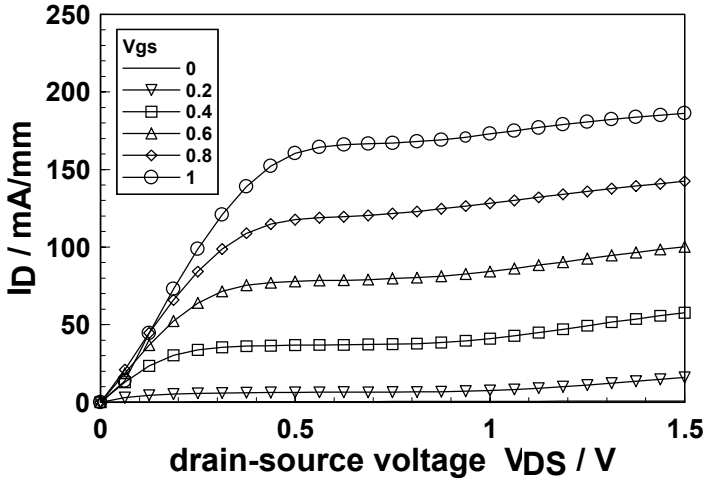


Fig. 2.5: Output characteristics of the enhancement type HFET(W_g = 30 µm, L_g = 1 µm).

WP 2.3 Experimental study on manufacturability

The InP-based RTD is investigated with respect to homogeneity and reproducibility. Three nominally identical runs are prepared as indicated above. Each consists of a quarter of a 2"-wafer. In Fig. 2.6 bar diagrams are given summarising the most important DC I-V-characteristic parameters with respect to digital circuit applications: peak-voltage and peak-current density. The average values for the peak-voltage and peak-current homogeneity are 2.3 % and 4.7 %.

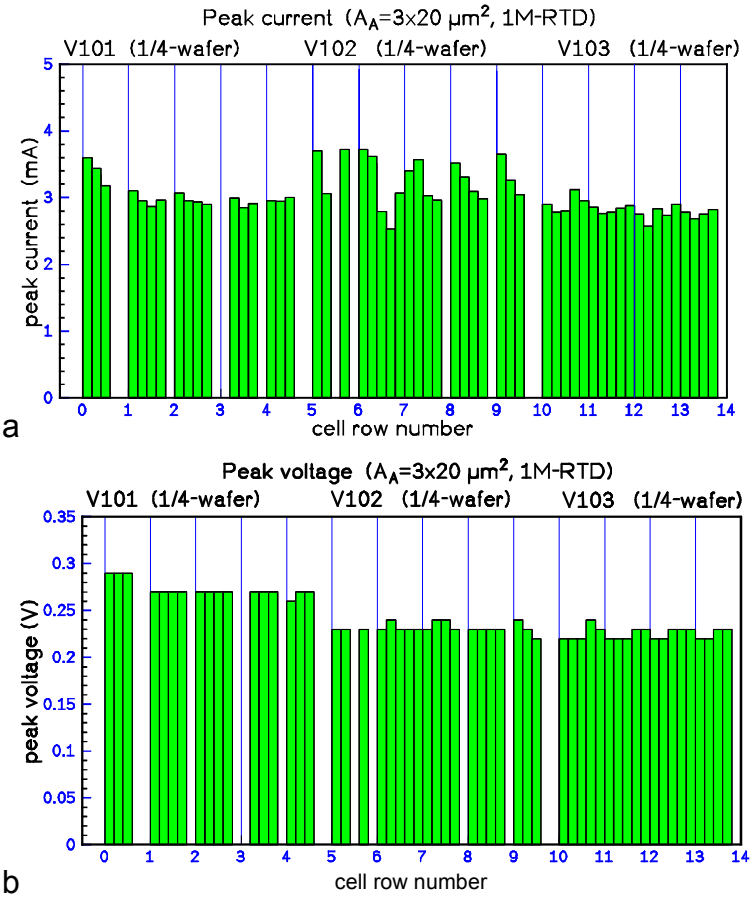


*Fig. 2.6: Experimental DC parameter variations of RTD in forward direction: (a) peak-current density, (**b**) peak-voltage.*

Small area devices (A_E = 10 µm² instead of 60 µm²) are also investigated in this study (cf. Fig. 2.7). The absolute peak-voltage is independent on the size of the device (cf. Fig. 2.7) and also the peak-voltage modifications are not affected. These data are mainly controlled by the epitaxial growth and should not be modified by the size of the device. In the case of substantial parasitic resistances such as contact and lead resistance, an additional voltage drop at high current densities might result in an increase of the peak-voltage, which is not observed here.

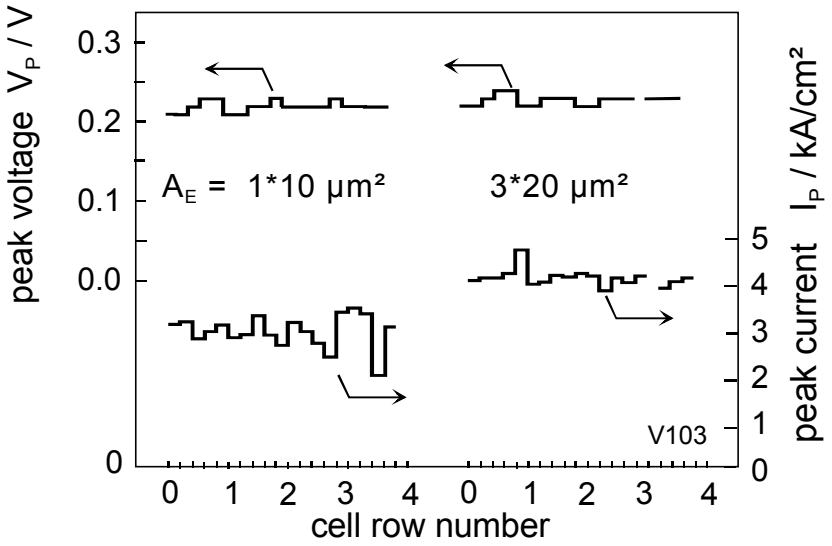


Fig. 2.7: Size dependence of experimental peak-voltage, and peak-current density variations of RTD in forward direction

The peak-current density and variation of small area devices, however, are clearly different from the larger ones. This effect is related to the reduction of the effective device area due to mesa under etching. A constant reduction of the lateral dimension (180 nm estimated) is more important for a small area device and this way an nominally lower peak-current density is calculated for the small area device. In addition, the modifications of lateral dimensions are also more important for the small area devices and typically twice the peak-current density modification is measured (cf. Fig. 2.7). If this increase is totally attributed to an inhomogeneity of lateral dimensions, a variation of 67 nm is calculated caused in our technology by lithography and etching.

These results clearly prove that MBE growth is capable of meeting the requirements for digital applications of RTD. Hence, the influence of layer data was overestimated in the past, especially if the device dimensions are shrinking according to low-power digital circuit applications [Chen et al. 1997]

WP 2.4: Demonstrator Circuits: NAND/NOR gates and multiple terminal LTGs

NAND/NOR gates

The first MOBILEs with three RTT input stages are realised on InP-substrate i.e. a NAND gate as shown in Fig. 2.8. The double barrier RTD as indicated above is grown on top of a InGaAs/InAlAs HFET within a single run by means of solid-source molecular beam epitaxy (MBE). This arrangement is necessary because any doped layer underneath the HFET would deteriorate its RF performance. Access to the buried RTD cathode is provided by a 5 nm n^{++}

InAlAs etch stop layer (cf. Fig. 2.4) which can be used for a selective citric acid etch process. The devices are fabricated by electron beam lithography. The mesa etching was carried out using a metal etching mask. A one layer PMMA resist (950k, 6% solids) was used for the main pattern steps. The ohmic contacts (Ge/Ni/Au) were annealed at T = 380°C for 10 s, achieving a contact resistance of below 0.1 Ωmm. The gates and connections are defined with the identical one-layer PMMA process. Subsequently, the gate recess is performed using a succinic acid based etchant followed by a Pt/Ti/Pt/Au-metallisation. The HFET gate length is 1 µm, the width 10 µm; the input RTD area is 3 µm². The threshold voltage is –0.09 V, the peak current density 9 kA/cm². Experimental results proving the gate functionality as a function of the input and clock frequency are shown in Fig. 2.8 for the critical logic input combinations of (1 0) = (0 1) and (1 1). The input and output levels are compatible so that no additional level shifters are needed.

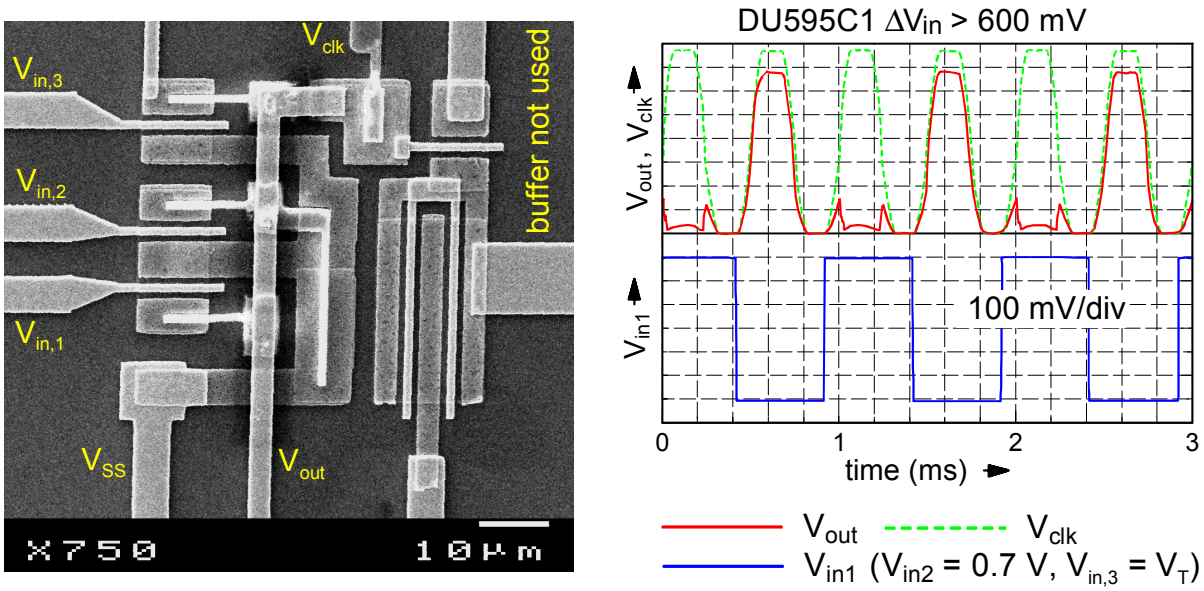


Fig.2.8: SEM picture of the MOBILE with three self-aligned RTT input stages and a buffer (left) and the clock, output and input voltages demonstrating the functionality of the novel concept.

Full Adder

The fabrication of the 1-bit Full Adder is scheduled as the final demonstrator of the LOCOM project. The design of this circuitry is presented in WP 1. In this section the layout and fabrication is given in detail. However, a successful demonstration of a full electrical functionality is still pending due to severe problems with the combined depletion and enhancement type HFET technology.

The epitaxial growth and fabrication of 3D-monolithically integrated pseudomorphic InP-based RTD-HDFET combinations are presented in WP 2.2 - 2.3. A progress is the novel gate-recess procedure using a solution of citric acid and hydrogen peroxide in a ratio of 2:1 and 1:10 for fabrication the depletion and enhancement type transistor, respectively. The first etchant removes InGaAs but stops on InAlAs, the second etches InGaAs and also lattice-matched InAlAs but stops on AlAs. This way the different recess depths can be adjusted by the almost perfectly controllable epitaxial layer thickness using a buried AlAs-layer in the lattice-matched InAlAs-barrier.

The layout of the basic building block, a RTD-HFET-HFET combination is given in Fig. 2.9. As a result from our HBT-research group dealing with contacting small emitter fingers, further advancements are achieved using 45° orientated RTD interconnection bridges (cf. Fig. 2.9 , left) or directly contacted RTDs (cf. Fig. 2.9, right). Since the etch-rate in the (100)- or (010)-direction is much higher than parallel to the fractured lines, in the first case the under-etching of the interconnection finger in order to isolate the anode from the contact pad is more efficient without seriously attacking the intended anode area. This way the size of the RTD anode area can be reduced to 1 µm² without loosing the functionality of the linear threshold gates (weighted by their anode areas) due to the better control of the effective anode area during the isolation etching. The advantage of direct contacted RTDs is that on one hand the effective anode area can be "perfectly" controlled since a "long" under-etch process can be omitted, on the other hand the effective size of a LTG can be drastically reduced since the supply connect run on polyimide over the active HFET area. Using the latter design small area full adders can be fabricated as shown in Fig. 2.10.

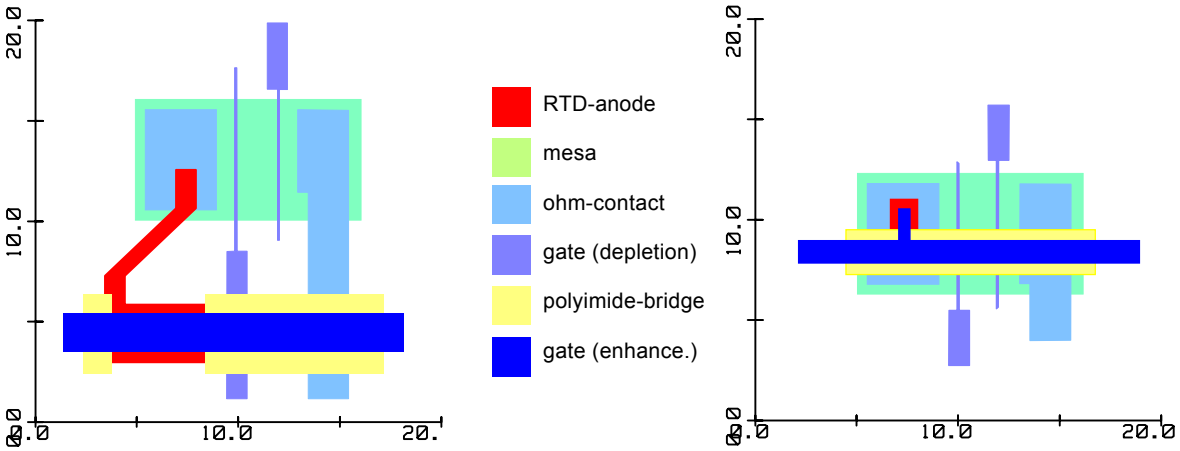


Fig. 2.9: Layout of a RTD connected via under-etched interconnection fingers (left hand) and of a directly contacted RTD using a polyimide bridge (right hand). The main orientation is parallel to the fractured lines (110) or (1-10), respectively, of the crystal direction.

The fabrication started with the evaporation of the RTD anode metal which also serves as a mask for the following etch step forming the RTDs. In a second etch step the HFET-mesas are defined while the RTD interconnection fingers are under-etched. After the evaporation and alloying of the HFET-source and drain contacts the depletion-type gates are fabricated. Polyimide is structured for the following final metal step completing the connection of the circuit and forming the enhancement-type gates. All process masks are e-beam written.
Fig. 2.11 shows the view from top left in Fig. 2.10 on a RTD-HFET input stage. The anode area is 1.5×2 µm² and connected via a 0.5 µm wide branch of the supply line running on polyimide (visible as shades) over two depletion-type gates with a length of 0.25 µm. Due to the under-etching of 180 nm the effective RTD anode area is less than 2 µm² leading to a peak current of 0.40 mA per input stage. The extrinsic transconductance of the HFET is 510 mS/mm.

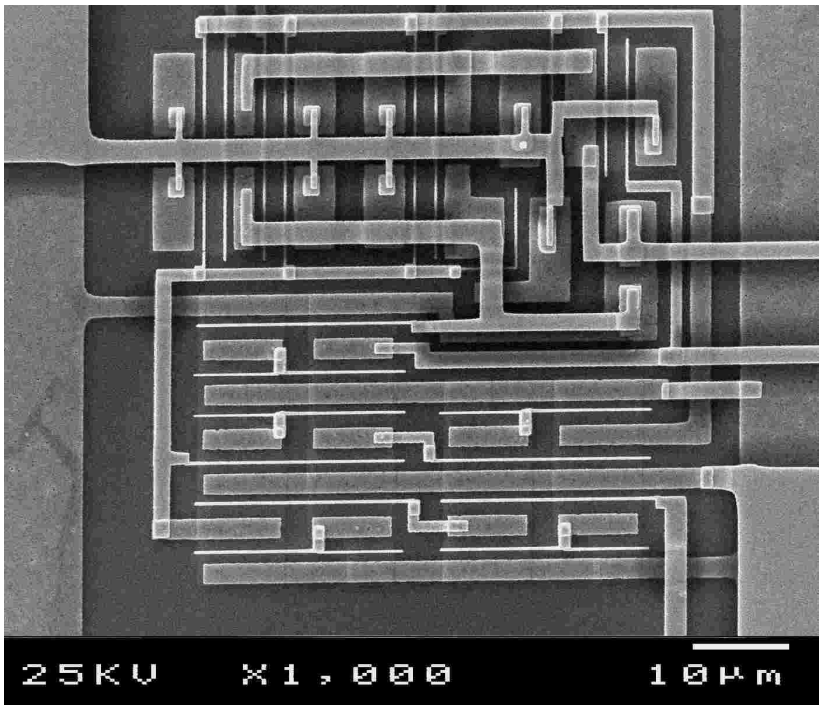


Fig. 2.10: Top view on a two stage threshold logic full adder with direct contacted RTDs. The bottom circuits (two SBFL inverter chains) generate the time-shifted clock signals for the carrier and sum circuit (cf. Fig 1.1a in WP 1).

Fig. 2.12 shows the technological realisation of the one-stage hybrid full adder with a Boolean pull-down path presented in Fig. 1.3b. The minimum gap between the connections are 2.5 µm due to proximity effects in the e-beam process. Using direct contacted RTDs and more metal layers for stacking the connections separated by polyimide, the area consumption of the whole circuit can be drastically reduced. Here the fabrication was focussed on a simple process with minimum step numbers in order to demonstrate the functionality of the adder concept based on LTG's.

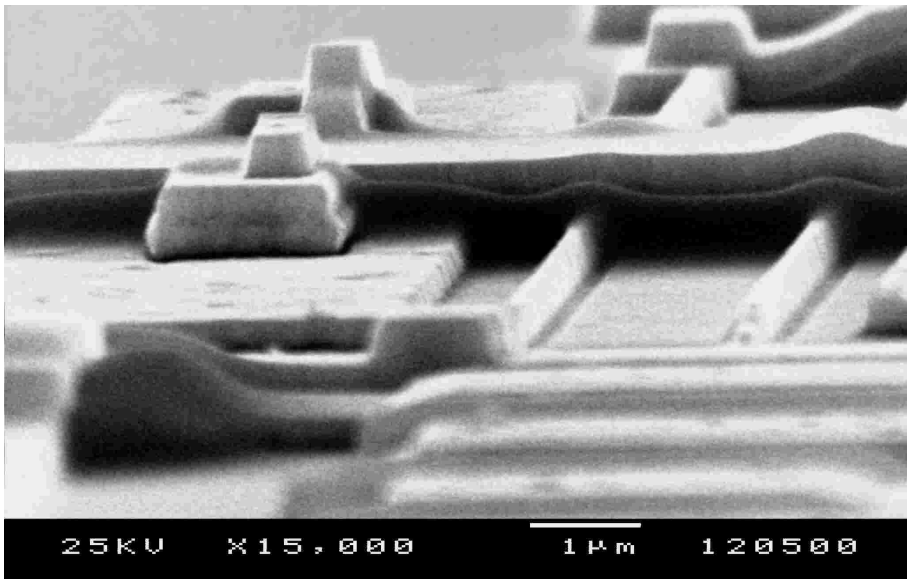


Fig. 2.11: Side view on the RTD-HFET input stage of the threshold logic full adder shown in Fig. 2.10. From left to right: self-aligned directly contacted RTD, gates of the clock and input transistor. The V_{DD}–line is leaded on polyimide bridges over the gates.

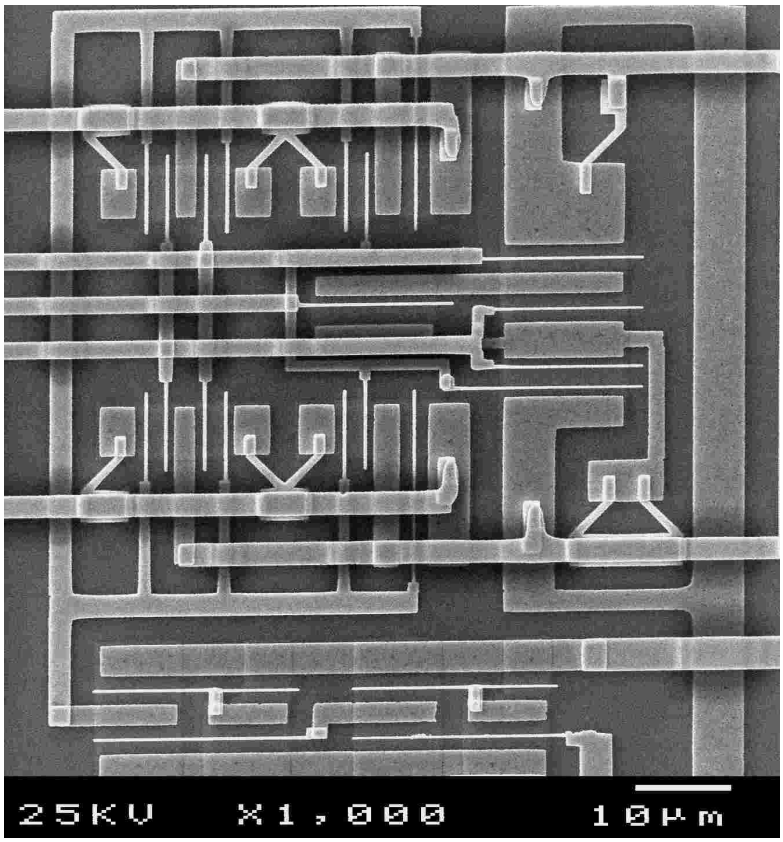


Fig. 2.12: Top view on the one-stage hybrid full adder combining threshold and boolean logic. From top to bottom: carrier computer, Boolean pull-down path with sum computer and the SBFL inverter chain for shaping the clock signal (cf. Fig. 1.1b).

I-V characterisation

The electrical functionality of the above presented technology is pending. In the following a short introduction is given in to the electrical measurement procedure. The output of an MOBILE type gate can drive a limited load, only. This load is far below a standard 50 Ω coaxial waveguide system for high speed electrical measurements. To the Full Adder circuit as given in Fig. 1.1 buffer amplifiers added. In Fig. 2.13 our approach is depicted. A super-buffer is designed and for clock delay purpose and in order to drive higher loads. Finally, a open-source type tapered buffer

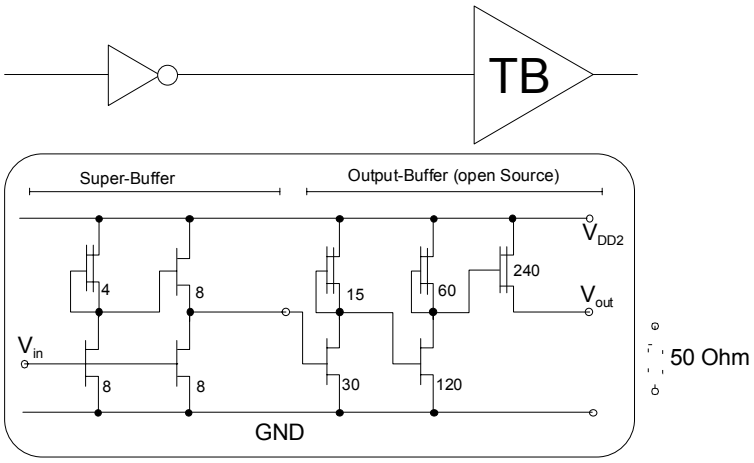


Fig. 2.13 : Buffer amplifier design for high-speed measurements. The 50 Ω load represents the coaxial waveguide measurement system.

is realised. This buffer amplifier is designed especially for a 50 Ω coaxial waveguide system. The electrical measurements are all done on-wafer with a probe-station and high frequency tips.

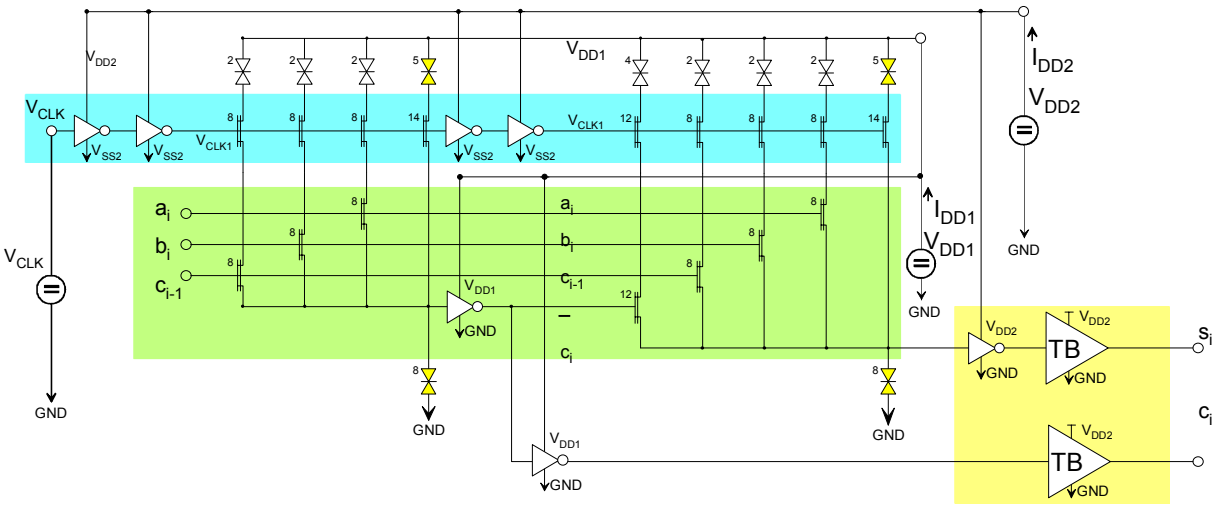


Fig. 2.14: Electrical measurement set-up for a preliminary analysis of circuit functionality ($V_{DD1} = V_{DD2} = 0.8$ V).

The electrical characterisation showed that the tapered buffers are not working properly due to problems with the e-beam lithography of large area exposures. Therefore, I-V measurements are performed in order to study the switching properties of the circuit. As an example a set-up for the analysis of the super-buffer is shown in Fig. 2.14 and the according I-V measurement is given in Fig. 2.15. At a clock voltage of 90 mV the super buffer output is switching indicated by a current peak I_{DD2}. As a consequence the super buffers in carry bit line are also switching and the transistor with 12 µm width is opened resulting in a higher current level. With a set of comparable measurements the chip is analysed and a proper function of the circuitry is found except the tapered buffer.

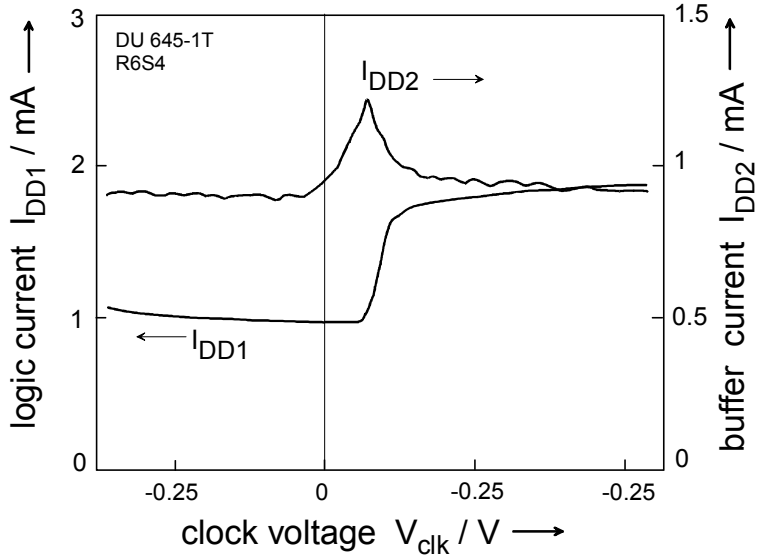


Fig. 2.15: I-V measurement for the analysis of the super buffer amplifier indicating a switching operation at 90 mV clock voltage.

WP 3: Device Simulation

Task 3.1 Parameter sensitivity in physical simulation

The existing program for the calculation of RTD I-V characteristics will be further developed for InP-based InAlAs/InGaAs structures. The material parameters for these structures are less accurately known than for GaAs/AlGaAs so calibration measurements are necessary on test structures. Especially the parameters for scattering have to be calibrated since they are difficult to be derived from basic theory.

Task 3.2 Layer structures with low parameter sensitivity

Based on the results of Task 3.1 structures will be designed where the parameter sensitivity is minimised. The dependence of structural parameters (thickness, composition) on process parameters (substrate and furnace temperatures, gas flows) will be taken into account and situations will be looked after where variation in one process parameter induces variations in structure parameters with opposing effects on the RTD characteristics.

Task 3.3 Si-NDR devices

The developments in the Si-based RTD field are being followed with an eye on NDR action at room temperature. The possibilities of strained Si or SiGe layers will be explored. In parallel the Esaki diode will be modeled and optimised for the present application.

WP3.1: Parameter sensitivity in physical simulation

In this workpackage the capability of modelling RTDs based on InP substrate consisting of InAlAs/InGaAs compounds had to be achieved. The calculation of the parameter sensitivity of RTDs requires a sufficiently good agreement between simulated and measured device characteristics. This could not be obtained with the already existing programs ARTICL from TUE and RTDSIM from GMUD which are originally designed for GaAs-based RTD devices. Therefore the two existing programs had to be revised for InP based RTDs with special emphasis to the I-V characteristics.

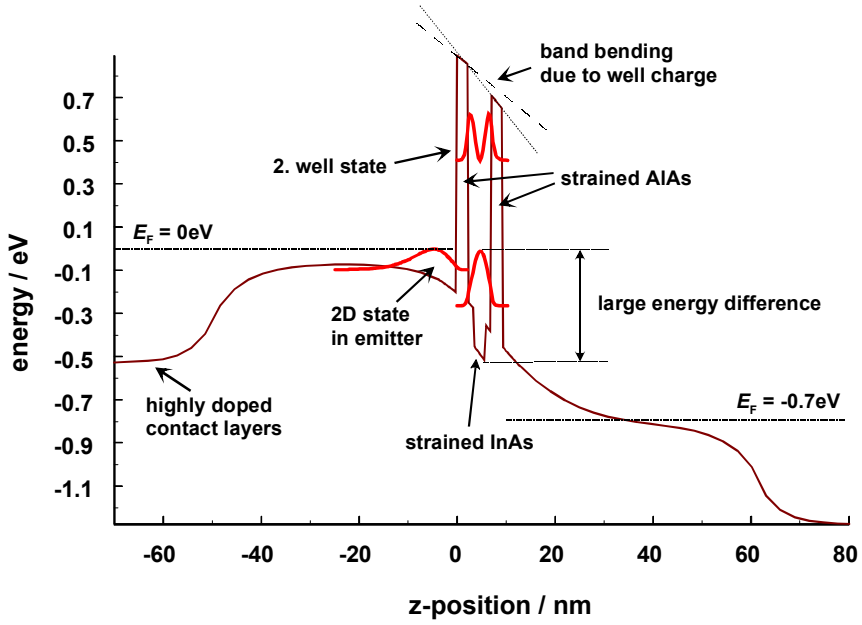


Fig.3.1: Conduction band profile of RTD device with applied bias voltage. Emitter 2D states, band bending due to well charge and deep subwell sketched.

Several effects in the RTD device made it necessary to modify the existing programs. Figure 3.1 shows an example conduction band profile of an InP-based RTD device with applied bias voltage that shows some of these effects. To achieve a better peak to valley current ratio the barriers are made of pure AlAs. A lower peak voltage can be obtained by using a low band gap subwell material. Unfortunately both induces strain, in the barriers that are now tensile strained and in the subwell that is now compressively strained on the lattice matched InGaAs layers. Due to the large strain of about ±3% the barriers are lowered and the well is lifted up again, contradictory to the intention and the effective masses in the Γ-valley become direction dependent. A second effect of the new materials related to the lower band gap compared to GaAs is the non-parabolic energy dispersion relation. Especially in the well this is important, because the higher energetic resonances in the quantum well are shifted to lower energies. On the other hand the barriers become much more transparent which increases the current density. Due to the very high contact doping concentrations the non-parabolicity has also an impact on the Fermi level of the contacts. An additional effect that is related to the lower doped contact regions next to the barriers is the formation of a 2D state in the emitter of the RTD at higher bias voltages. Alignment of this 2D state with a resonance in the well leads to a sharper and higher current peak compared to the peak of the continuum reservoir. In the following paragraph we want to explain how the new effects are modeled and what the new material parameters in our material system are. After that we describe the two existing programs.

The materials we are using are $In_{1-x}Ga_xAs$ and $In_{1-x}Al_xAs$ compounds on a InP substrate. A description of the conduction band edge at 300K relative to the conduction band energy of $In_{0.53}Ga_{0.47}As$ is found with a quadratic polynomial that is fitted to the conduction band energies of the binary compounds and the lattice matched compounds $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ (see [Chuang95] for material data):

$$E_C\left(\mathrm{In_{1-x}Ga_xAs}\right) - E_C\left(\mathrm{In_{0.53}Ga_{0.47}As}\right) = -0.28\mathrm{eV} + 0.4086\mathrm{eV}\cdot x + 0.398\mathrm{eV}\cdot x^2 \qquad (3.1)$$

$$E_C\left(\mathrm{In_{1-x}Al_xAs}\right) - E_C\left(\mathrm{In_{0.53}Ga_{0.47}As}\right) = -0.28\mathrm{eV} + 1.4426\mathrm{eV}\cdot x + 0.38\mathrm{eV}\cdot x^2 . \qquad (3.2)$$

The band gap energies of the unstrained materials can be modeled in the same way:

$$E_G\left(\mathrm{In_{1-x}Ga_xAs}\right) = 0.354\mathrm{eV} + 0.641\mathrm{eV}\cdot x + 0.429\mathrm{eV}\cdot x^2 \qquad (3.3)$$

$$E_G\left(\mathrm{In_{1-x}Al_xAs}\right) = 0.354\mathrm{eV} + 1.921\mathrm{eV}\cdot x + 0.755\mathrm{eV}\cdot x^2 . \qquad (3.4)$$

Also the effective masses are modeled with quadratic polynomials:

$$m^*\left(\mathrm{In_{1-x}Ga_xAs}\right) = 0.021\mathrm{m_0} + 0.031\mathrm{m_0}\cdot x + 0.011\mathrm{m_0}\cdot x^2 \qquad (3.5)$$

$$m^*\left(\mathrm{In_{1-x}Al_xAs}\right) = 0.021\mathrm{m_0} + 0.085\mathrm{m_0}\cdot x + 0.04\mathrm{m_0}\cdot x^2 . \qquad (3.6)$$

Effects due to strain in the (001) plane of our zincblende semiconductors can be described by the deformation potential theory [Pollak90]. Especially the Γ-valley is only dependent on the volume dilatation, because only strain components in the main axis directions of the crystal exist. We obtain a simple shift of the conduction band energy [Chuang 95, Köpf 97,Ohler 98]:

$$\Delta E_C = a_C\left(e_{xx} + e_{yy} + e_{zz}\right) \qquad (3.7)$$

$$\text{with} \qquad e_{xx} = e_{yy} = \frac{a_{substrate} - a_{layer}}{a_{layer}} \qquad (3.8)$$

and $$e_{xx} = -\frac{2c_{12}}{c_{11}} e_{xx} \,. \tag{3.9}$$

Here e is the strain tensor with its components along the main axis directions and a_C is the deformation potential. The used elastic stiffness tensor elements are c_{11} and c_{12}. Following Vegard's Law the lattice constants a and the elastic stiffness tensor elements of the compound layers can be calculated with a linear approximation:

$$a\left(A_x B_{1-x} C\right) = a_{AC} x + a_{BC}(1-x) \,. \tag{3.10}$$

Additionally the band gap energy is also shifted due to the strain. Unfortunately the three valence bands of the light, heavy and split of band holes are shifted into different directions and by different values. Fortunately their average energy is shifted like the conduction band energy, according to equation (3.7), with a deformation potential a_V. So the average band gap shift can be modeled with:

$$\Delta E_G = \left(a_C - a_V\right) \cdot \left(e_{xx} + e_{yy} + e_{zz}\right), \tag{3.11}$$

which is accurate enough for our calculations. The impact of the strain on the effective masses is connected to the change of the band gap energies. In the **k·p** theory the following relation for the conduction band effective mass in the Γ-valley is derived:

$$\frac{1}{m^*} = 1 + \frac{E_P}{3}\left(\frac{2}{E_G} + \frac{1}{E_G + \Delta_0}\right), \tag{3.12}$$

where E_P is the squared conduction to valence band momentum matrix element and Δ_0 is the energetic distance of the split of band from the valence band maximum. Unfortunately the effective masses perpendicular and in parallel to the layer interfaces suffer from a different change but fortunately the change is in the same direction and the new masses can roughly be calculated by the following method: 1) calculate E_P from the unstrained values, 2) determine the new average band gap energy, 3) calculate the strained mass using equation (3.12) and the new band gap energy. A better fit for the $In_{1-x}Ga_xAs$ material grown on InP is given in [Köpf97] with:

$$\begin{aligned} \frac{m^*_{x,y}}{m_0} = \frac{m^*}{m_0} &+ \left(-0.319 + 0.132x - 0.147x^2\right) e_{xx} \\ &+ \left(-3.65 + 11.21x - 7.6x^2\right) e_{xx}^2 + \left(-10.5 + 164.0x - 67.85x^2\right) e_{xx}^3 \end{aligned} \,, \tag{3.13}$$

$$\begin{aligned} \frac{m^*_{z}}{m_0} = \frac{m^*}{m_0} &+ \left(-0.33 - 0.168x + 0.104x^2\right) e_{xx} \\ &+ \left(-2.1 - 0.593x + 1.692x^2\right) e_{xx}^2 + \left(-25.86 - 57.81x + 61.56x^2\right) e_{xx}^3 \end{aligned} \,. \tag{3.14}$$

material	a_0 / nm	$-2\,c_{12}/c_{11}$	Δ_0 / eV	a_C / eV	a_V / eV
AlAs	0.5660	-0.8544	0.28	-5.64	2.47
GaAs	0.5653	-0.9051	0.34	-7.17	1.16
InP	0.5869	-1.1098	0.11	-5.04	1.27
InAs	0.6058	-1.0868	0.38	-5.08	1.00

Tab.3.1: Material parameters for the InGaAs and InAlAs material system on InP substrate

where e_{xx} is the strain in parallel to the interfaces (s. eq.(3.8)) and x is the Gallium-fraction. The parameters needed to calculate all the band gaps and strain shifts are given in table 3.1. As previously mentioned the parabolic energy dispersion relation does lead to wrong results for the peak voltage due to the low band gap materials in the well. Instead we use the energy dispersion relation presented by [Kane57]:

$$E \cdot (1 + \alpha \cdot E) = \frac{\hbar^2 k^2}{2m^*}, \tag{3.15}$$

$$\text{with} \quad \alpha = \frac{1}{E_G}. \tag{3.16}$$

E is positive in the conduction band and negative in the band gap. Note that negative values of E lead to imaginary wave vectors k which means the mode is attenuated and not propagated. A graphical presentation of the parabolic and non-parabolic energy dispersion relations is given in figure 3.2.

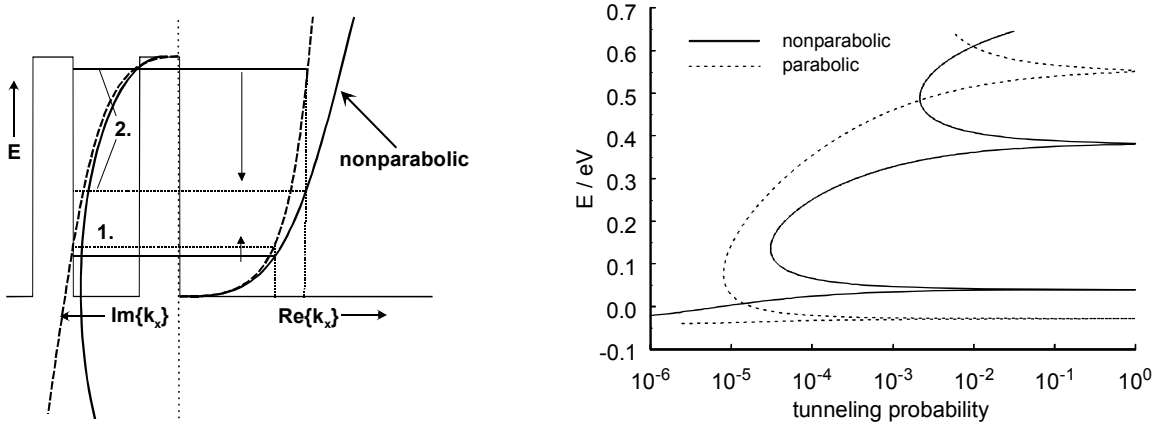


Fig.3.2: Comparison of the parabolic (dashed) and non-parabolic (solid) energy dispersion relations (left) and the impact on the tunnelling probability at 0V (right).

The second resonance is shifted to a lower energy which means the width of the valley in the I-V characteristic becomes smaller. The first resonance is shifted to a higher energy, so the peak voltage is larger than calculated with a parabolic energy dispersion relation. This is an effect of the lower attenuation of the barriers. An additional effect of the new energy dispersion relation is a slightly different calculation method of the electron density for high Fermi levels.

In the following paragraphs we will describe our two simulation programs. Both programs calculate the RTD current in one dimension which is the growth direction. This is sufficient since the lateral dimensions of our RTDs are large enough and quantum effects are only expected in the growth direction. The potential and charge distributions of the whole structure are calculated by iterative, self-consistent methods. Both use the transfer matrix method to calculate the transmission probabilities.

RTDSIM program description:

Since the doping levels of the contact layers are very high in our RTDs the Fermi levels in the emitter and collector can be assumed as constant. The calculation of the charge is divided into a simple calculation using the Fermi-Dirac statistics near the contacts and a calculation based on 2D electron states in regions where the quantum effects occur. Quantum effects mainly occur in the quantum well between the two potential barriers and in the contact regions next to the barriers, especially in the emitter where a quantum well is formed at high voltages. The quantum charges in the emitter are calculated by using a finite difference discretisation of the time

independent Schroedinger equation and solving for all eigen-values and eigen-functions using subroutines from the free EISPACK algebra library. The important difference to the ARTICL program is that there is no distinction between 3D- and 2D-charge in this region. All the charge is 2D. Figure 3.3 (left) shows all eigen-functions calculated with this method for an example potential profile. One bound state in the emitter and one state in the well are visible.

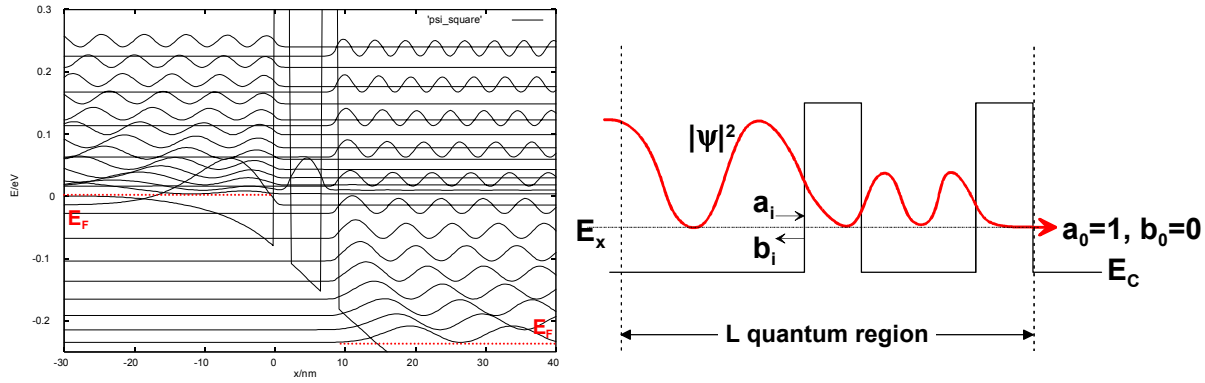


Fig.3.3: Wave functions calculated with the 1D Schroedinger equation solver (left), example wave function for 2. resonant state in the quantum well propagated from the right to the left contact region (right)

A wave propagation method is used to calculate the tunnelling probabilities and the well charge of the intrinsic RTD layer stack. Figure 3.3 (right) shows an example shape of a squared wave function. We assume that the collector states do not affect the well and emitter electron states. Therefore we start at the right side of the collector barrier with an arbitrary wave amplitude of a_0=1 assuming plane forward and backward propagating electron waves in every discretisation point. There is no reflection assumed (b_0=0). Using the transfer matrix method we can calculate the wave amplitudes of every discretisation point left of our starting point. We have introduced a damping inside the well that is a fitting parameter and describes the loss of coherently tunnelling electrons due to scattering events. The complex tunnelling and reflection probabilities are now simply t=1/a_i and r=b_i/a_i. Normalisation of the resulting wave function $|\Psi|^2$ and integration over k-space leads to the electron density at every discretisation point. Integration over the half k-space at the sketched point i and taking into account the tunnelling probability gives the current density in one direction. If the quantum region is extended far into the emitter region, we automatically take into account the coupling of emitter and well states. If we introduce scattering in the well the equation $|t|^2+|r|^2=1$ is no longer valid. From $1-|t|^2-|r|^2$ we can calculate the incoherent tunnelling probability through our double barrier structure assuming the scattered electrons are collected in the well at their injection energy and tunnel out to both sides proportional to the tunnelling probabilities of the two single barriers. From the incoherently tunnelled electrons we can determine the value of the incoherent electron charge inside the well by using the tunnelling probability of the collector barrier. The shape of the electron distribution is the same as previously calculated only different by a constant factor. Coupling effects between electrons in the Γ and the X valleys of the Brillouin zone are not expected for our RTD materials. This coupling can be significant for AlAs/GaAs structures but is minor for InAlAs/InGaAs structures. The device capacitance can be calculated by two simulations with a differential small voltage step. We determine the total capacitance from the maximum of the difference quotients of the electron charges in the emitter and the collector and the total applied voltage.

$$C = \max\left(\frac{dQ_{\text{collector}}}{dV}, \frac{dQ_{\text{emitter}}}{dV}\right) \tag{3.17}$$

ARTICL program description

Most of the calculation methods used in RTDSIM are equal to the methods used in ARTICL. Nevertheless there are differences. The emitter region is modeled by a modification of the SCALPEL program of IMEC Leuven [Hendriks96]. Here the emitter region is divided into two parts, divided by the maximum of the conduction band. To the left it is assumed that all electrons are in 3D states, to the right a potential well exists in which 2D levels can occur. Above the conduction band maximum only 3D states are assumed to exist. In the transfer matrix method Γ-X coupling can be included with a coupling factor that is treated as a fitting parameter. Scattering is represented by adding an imaginary part to the potential in regions where real *k*-values are expected, i.e. in the well for Γ-electrons and in the barriers for X-electrons. The damped wavefunctions represent the loss of coherent electrons in the well. The incoherent electrons are supposed to tunnel out through both barriers proportional to the respective transmission probability. Charge in the well is calculated from the wavefunctions in the well for both coherent and non-coherent tunnelling. Because the ARTICL program originally allows only one well layer we extended the program code to take into account a subwell layer that is centered in the original well layer. The kinetic electron energy is always positive in this layer. Since ARTICL assumes a constant conduction band energy in the well layer the subwell layer can be modelled by a phase shift of the electron wave. Reflections are negligible because of the high kinetic energy in the well. The voltage drop over the collector region is calculated self-consistently assuming that the charge of the tunnelling electrons is negligible compared to the electrons back-diffusing from the highly doped contact region. Since the charges in both emitter and quantum well are calculated it is also possible to calculate the capacitance of the device. For AlGaAs/GaAs devices this has yielded good agreement with values extracted from microwave impedance measurements.

Comparison with experiments

After applying the modifications to both programs we tried to fit our simulation results to the measured I-V characteristic of our standard RTD device DU644 (s.fig.2.4) to have a starting point for the sensitivity analysis. For both programs we had to lower the height of our strained AlAs barriers from 1.25eV as calculated with the material formulas to 0.81eV to get the fit shown in figure 3.4 (left).

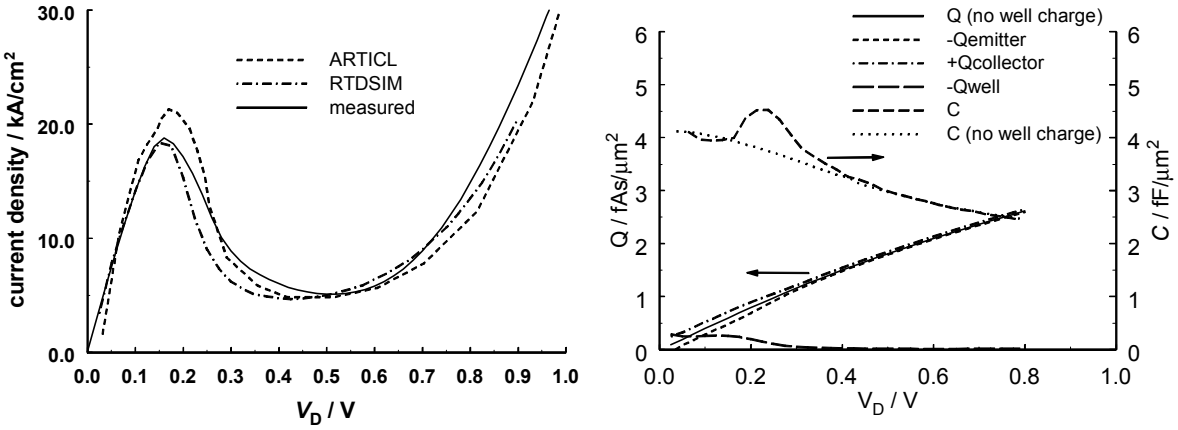


Fig.3.4: Comparison of the simulated and measured I-V characteristics of our standard device (left), simulated device charges and capacitance (right)

This was also necessary for other RTDs with strained pure AlAs barriers or strained barriers with a high Al content. In [Broekaert88] a RTD similar to our standard RTD is presented but they assume a barrier height of 1.11eV. One explanation for the lower barrier could be that the strain induces a dipole plane so that the discontinuities have different values than expected. Another explanation could be the indirect band gap of the barrier material. Nevertheless with the right choice of the fitting parameters also the valley current densities are correctly modeled. In the

RTDSIM program the damping of the electron wave per length Δx due to scattering was assumed to be $e^{-0.0725/\mathrm{nm}\cdot\Delta x}$. Since the emitter, well and collector charges are calculated we can determine the total capacitance of the device as show in figure 3.4 (right). The well charge causes a dip in the emitter charge and a hump in the collector charge and this causes a peak in the device capacitance located at the steepest point of the NDR-region.

WP 3.2: Layer structures with low parameter sensitivity

To find a layer structure with low parameter sensitivity we started with the sensitivity analysis of the structural device parameters as barrier width, doping concentration and length of the low doped contact layer, subwell width, smoothing layer width and spacer width. The major results of our sensitivity analysis for DU644 performed with RTDSIM were that the barrier width has exponential impact on the current density as can be seen in figure 3.5 (left). The nominal value of 8ML for the barrier width should not be smaller because then the area of the RTDs in our circuits has to be too small so that we can not fabricate the RTDs in a reliable way because of under etching effects.

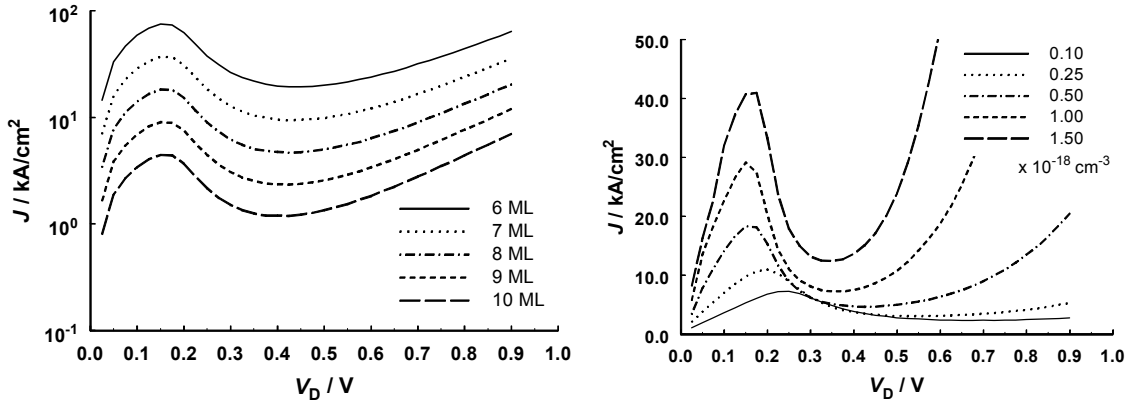


Fig.3.5: Current density in dependence on the barrier width in mono layers (nom. 8ML) (left) and in dependence on the contact layer doping (nom. $0.5\cdot10^{18}cm^{-3}$) (right)

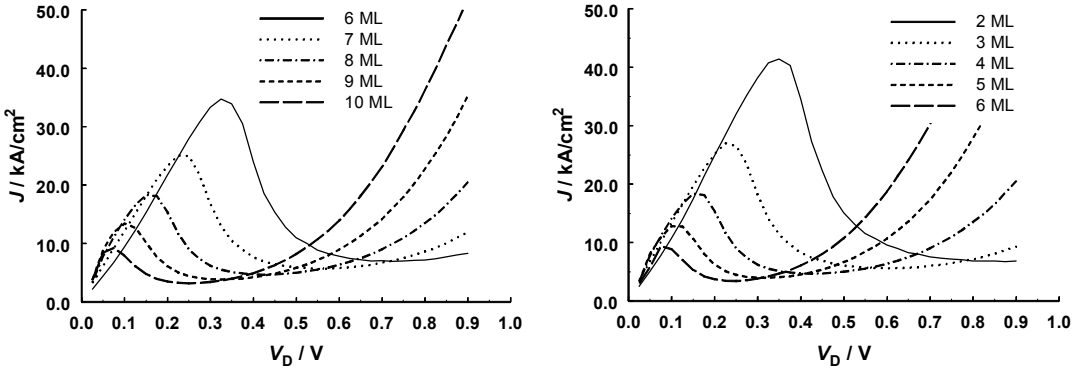


Fig.3.6: Current density in dependence on the subwell width (nom. 8ML) (left) and smoothing layer width (nom. 4ML) (right).

But also the doping of the contact layers has much influence on both the current density and the peak voltage (s.fig.3.5 (right)). A low peak voltage is desirable but a higher contact doping than $0.5\cdot10^{18}cm^{-3}$ would not further decrease the peak voltage. It would only increase the peak current density and decrease the peak to valley current ratio. The subwell and smoothing layer width has much influence on the peak and valley voltages as presented in figure 3.6. Note that there is a

smoothing layer next to each side of the subwell, so the impact of the smoothing layer seems to be larger. Wider subwell and smoothing layer width than 8ML for the subwell and 4ML for the smoothing layers each could decrease the peak voltage and peak current density and would allow us to use larger RTD device areas, but the peak to valley current ratio would be lower, too. Other structural parameters with less impact on the I-V characteristic are the spacer layer width and the width of the low doped contact layers. The spacer layer has only a small impact on the I-V characteristic (s.fig.3.7 (left)) so that we prefer the nominal value of 4ML for our RTD structure with minimum parameter sensitivity. Our simulation results in figure 3.7 (right) shows that the width of the low doped contact layers is only important if it is smaller than the depleted region, in our case for l<50nm which is already the nominal value.

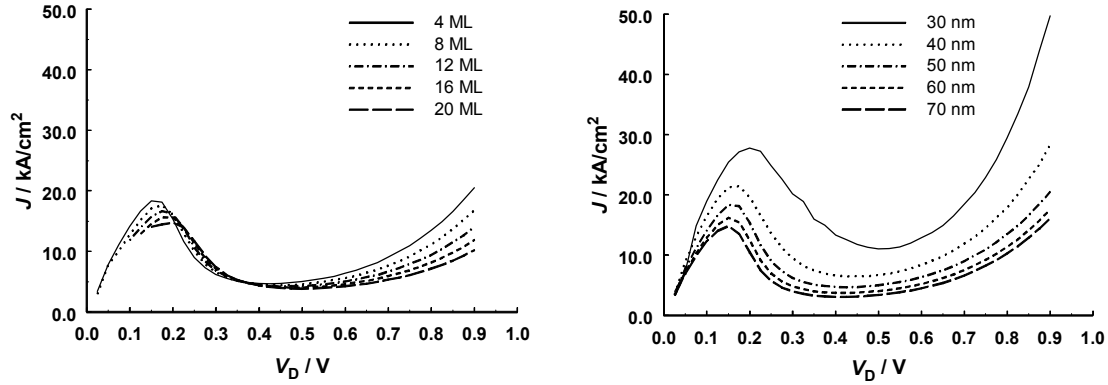


Fig.3.7: Dependence on the spacer layer width (nom. 4ML) (left) and low doped contact width (nom. 50nm) (right)

All these investigations let us conclude that we already have an optimised structure for our logic circuit RTDs. That is no surprise since the standard structure is the result of a previous experimental based optimisation. The sensitivity results for the different structural parameters are extracted from the simulation results in figures 3.5-3.7 and are summarised in table 3.2.

Parameter	nom. Value	sensitivity dJ_P/dParameter	sensitivity dV_P/dParameter
$d_{barrier}$	2.19 nm	-47.46 kA / cm^2 nm	-0.1 mV / nm
$d_{subwell}$	2.51 nm	-18.60 kA / cm^2 nm	-223.5 mV / nm
$d_{smoothing}$	1.17 nm	-24.20 kA / cm^2 nm	-204.5 mV / nm
d_{spacer}	1.17 nm	-0.60 kA / cm^2 nm	12.8 mV / nm
$d_{contact}$	50 nm	-0.26 kA / cm^2 nm	4.3 mV / nm
$N_{contact}$	5x10^{17}cm^{-3}	24.26x10^{-18} kA cm	-46.7x10^{18}mV cm^3

Tab.3.2: Parameter sensitivities of the structural RTD parameters of probe DU644 calculated with the RTDSIM program

The influence of the structural parameters on the device capacitance was also investigated. The contact doping showed the largest impact on the capacitance because it determines the width of the depletion region (s.fig.3.8 (left)). Surprisingly, symmetric variations of the barrier thickness did not change the overall charge in the well nor the height of the capacitance peak as shown in figure 3.8 (right). If the collector barrier is wider than the emitter barrier the well charge and the capacitance peak is larger, in the other case the well charge and the peak are lower than in the symmetric case.

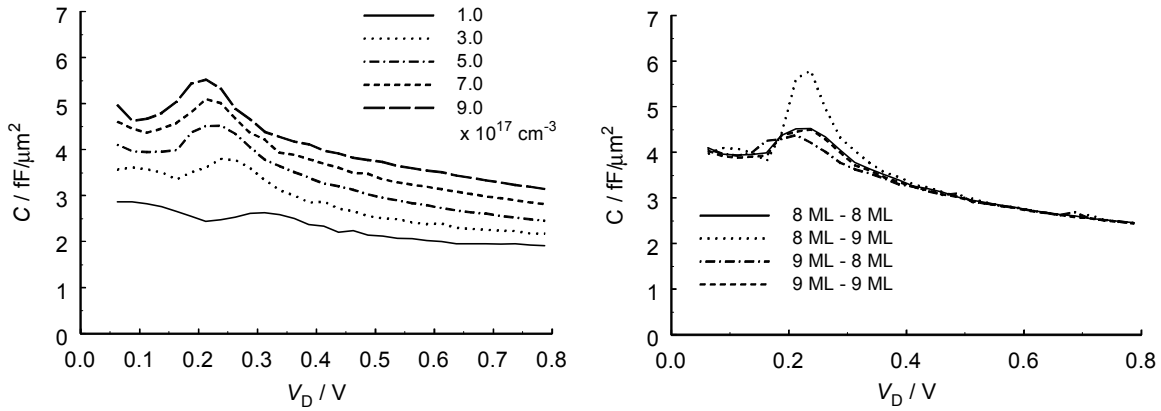


Fig.3.8: Dependence of the device capacitance on the doping concentration of the low doped contact layer (left), impact of symmetric and asymmetric barrier width variations on the device capacitance (right)

WP 3.3: Si-NDR devices

Since Si/Ge-RTDs do not work properly at room temperature because of their indirect band gap and the low barrier height, the NDR-device of the choice in the Si-material system is an interband tunnelling diode. Simulation of interband tunnelling devices is difficult [Kane61] because we have to include more than one band in our calculations. Especially the valence band structure is very complicated. To reduce the effort in the calculations we limited the model to one conduction band and one valence band. The charge in the valence band is calculated with the heavy hole data. The simulation program uses the 1D-poisson equation and the Fermi-Dirac equation in an iterative scheme to calculate the potential and the charge density inside the device. 2D-states in the quantum wells caused by the δ-doping are iteratively and self consistently calculated by solving a 1-dimensional discretisation of the Schroedinger-equation with the eigen-value and eigen-function routines of the EISPACK math library. The continuity equation and the current calculation are not included and we assume a step in the Fermi level located in the middle of the undoped tunnelling layer. This enables us to calculate at least the depletion capacitance of the device. For devices with high current density we expect an additional capacitance contribution $C_{\text{injection}}$ similar to the diffusion capacitance in normal pn-diodes. This contribution may have its origin in the injection of holes to the n-side and electrons to the p-side of the device due to tunnelling. A suitable model similar to the diffusion capacitance model in [Fjeldly98] would be:

$$C_{\text{injection}} = \tau \cdot g_{\text{P}} \ , \tag{3.18}$$

where τ is a time constant and g_{P} the intrinsic diode conductivity. By applying this model to extracted capacitance data of measured ITDs we could transform the extracted, v-shaped, intrinsic capacitance C_{P} of probe S1408 (A=60µm^2) into the normal monotonically increasing shape of a depletion capacitance as presented in figure 3.9 (left). The time constant was τ=5ps. Probe S1393 did only show the depletion capacitance behaviour because the current density of this device was 40 times lower.

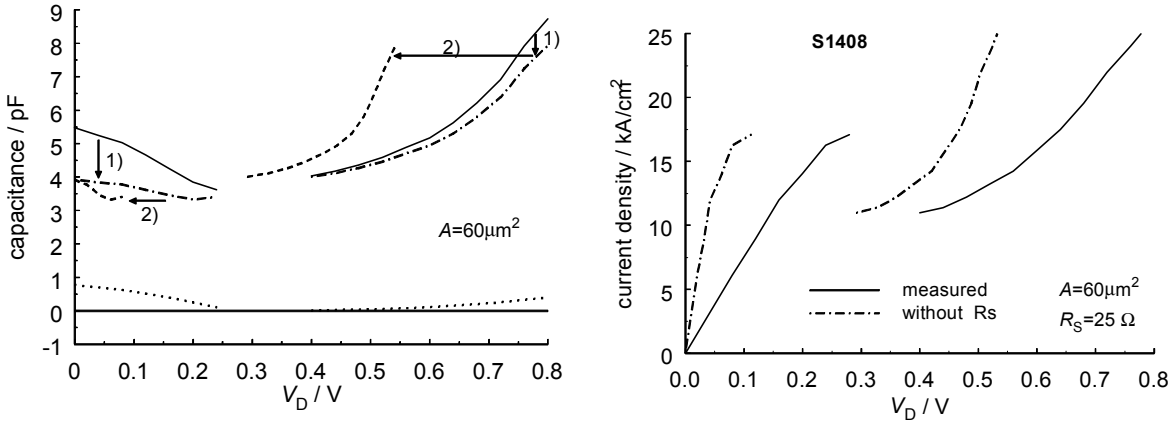


Fig.3.9: Transformation of the measured capacitance of probe S1408 into a depletion capacitance shape: 1. subtracting the diffusion capacitance (τ=5ps), 2. left shift due to series resistance, (right) measured I-V characteristic, NDR not stable

Two different layer structures were investigated in our simulations. One ITD consisting of Si only and a second with a $Si_{0.52}Ge_{0.48}$ tunnelling layer inserted. The contact layers had a doping concentration of $5x10^{19}cm^{-3}$ for the n-contact and the p-contact. The δ-doping densities are $10^{14}cm^{-2}$ for the n-side and p-side, respectively. A 4nm undoped Si tunnelling layer is the heart of the Si-only device, while the SiGe-device has a tunnelling layer consisting of 1nm Si at the n-doped contact followed by 3nm $Si_{0.52}Ge_{0.48}$ (s. detailed info. Duschl 00]). Figure 3.10 shows the band diagrams of our ITDs with applied bias voltage.

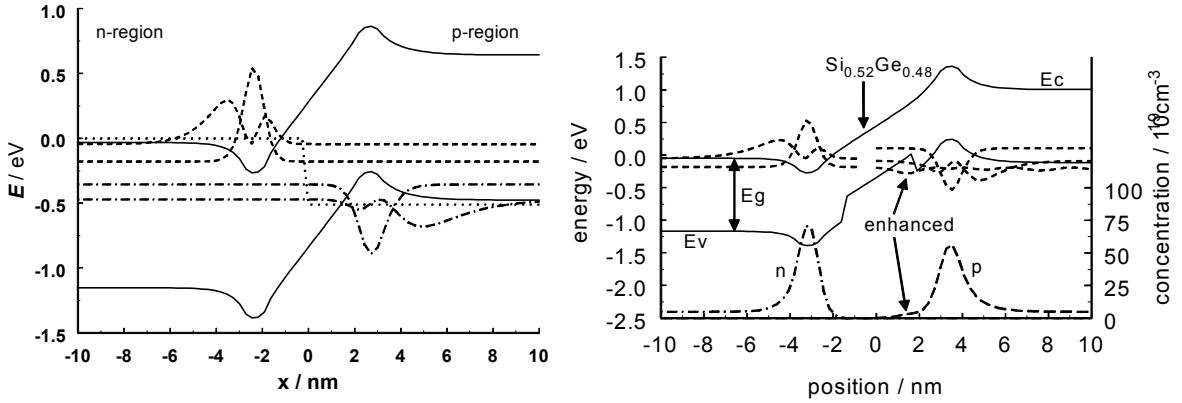


Fig.3.10: Band diagram of pure Si-ITD (V_D=0.5V) (left) and SiGe-ITD-device (right) with applied bias voltage (V_D=0.2V), including electron and hole 2D-states as well as electron and hole concentrations

2D-states can be found in the δ-doped regions. The δ-doping is modeled as 1nm wide layers with a doping concentration of $10^{21}cm^{-3}$. The tunnelling layer in the right diode consists of $Si_{0.52}Ge_{0.48}$ that is grown strained on the Si substrate. $Si_{1-x}Ge_x$ compounds do not have a significant conduction band offset and all the band gap difference is accumulated in the valence band. So the hole charge can move closer towards the n-region (s.fig.3.10 right) and therefore we expect an increased device capacitance. On the other hand the tunnelling layer becomes much thinner and the current density higher. We also expect a strong band gap narrowing effect in the δ-doping layers in the order of 0.1eV [Palankovski 99, Souifi 93]. Figure 3.11 shows simulation results of the capacitance voltage characteristics of our example ITD structures.

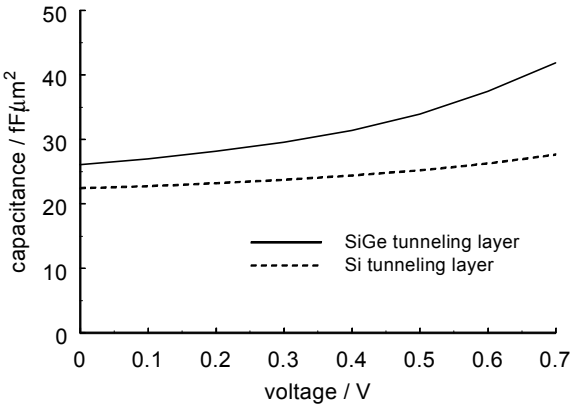


Fig.3.11: Calculated capacitance-voltage characteristics of the SiGe- and Si-only ITDs

The device capacitance at 0V is about five times higher than for RTDs with the same current density, e.g. DU644, because the tunnelling layer is much thinner. Unfortunately the simulated capacitance is 2 times lower than the extracted one of S1408. But the values of S1393 are close to the simulation data. Possible reasons are the omitted light holes in our simulations or wrong band gap data. Nevertheless, in figure 3.11 we find an increasing capacitance with increasing bias voltage since we are in the forward direction of the pn-diode. Furthermore the capacitance of the SiGe-device is larger than the capacitance of the Si-only ITD.

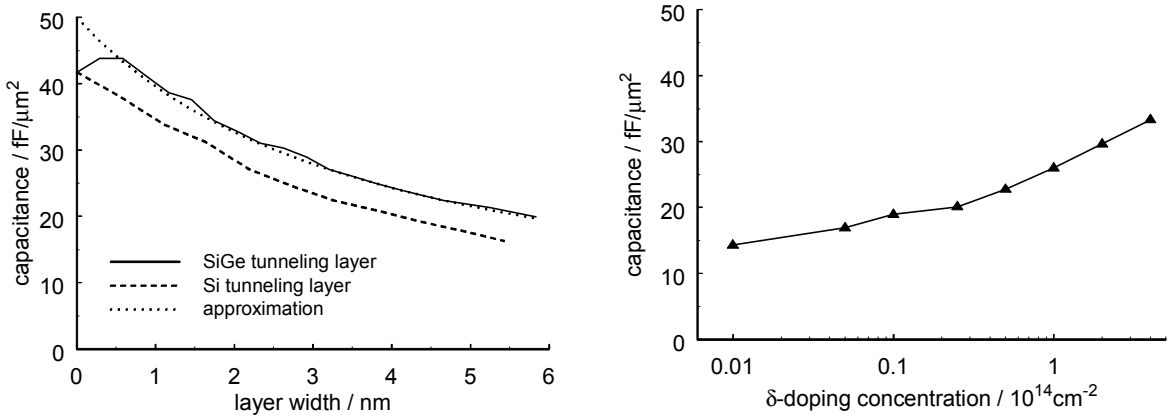


Fig.3.12: Capacitance at 0V in dependence on the tunnelling layer width (left) and of the SiGe-diode in dependence on the delta-doping density (right)

The impact of structural parameters on the capacitance was investigated with device simulations. Our calculations of the capacitance at V_D=0V showed that the contact doping has no influence because the charge is screened by the δ-doping. A major impact on the capacitance has the width of the tunnelling layer. Fig. 3.12 (left) shows the device capacitance as a function of the Si and SiGe tunnelling layer, respectively. The approximation for the SiGe-ITD drawn in figure 3.12 (left) represents the capacitance of a series connection of two capacitances, one constant and one that is reciprocal to the SiGe tunnelling layer length l:

$$C(l) = \frac{1}{\frac{1}{50\,^{\mathrm{fF}}/_{\mu\mathrm{m}^2}} + \frac{1}{\frac{650\,^{\mathrm{fF}}/_{\mu\mathrm{m}^2}\,\mathrm{nm}}{l}}}. \tag{3.19}$$

Lower δ-doping values may lead to a lower overall capacitance as presented in figure 3.12

(right), but this would decrease the current density as well. At high δ-doping concentrations the capacitance follows a logarithmic law.

We have to expect a higher capacitance for ITD-devices than for RTDs with the same peak current density, which may limit the RF-behaviour in our circuits. On the other hand this characteristic may be useful for memory applications, because it could decrease the refresh frequency if the valley currents are small enough. Since the current is exponentially decreasing with increasing tunnelling layer and the capacitance is only reciprocally decreasing in the same time, making the tunnelling layer too wide means increasing the internal time constant for charging and de-charging.

WP 4: Evaluation of Manufacturability

Task 4.1 Device level tolerance

The sensitivity of the RTD characteristics, particularly the peak and valley currents and densities, to variations in technological parameters like layer thickness and compositions will be studied in detail. Input data to these simulations are material homogeneity and reproducibility data from task 2.1. The impact of these tolerances on the devices are computed and give advice for a fault tolerant device design. In addition, the device tolerances are compared with experimental homogeneity and reproducibility data.

Task 4.2: Circuit level tolerance

The investigation of the circuit level tolerance includes the analysis of critical electrical device parameters, potential failure models and the fault tolerance of the threshold logic circuit design style. The deviations of the electrical device parameters from their nominal value and the local device mismatch will be classified concerning their consequences for the circuit design (logic voltage levels, fan-in) by means of the “GAME“ simulator, a SPICE add-on tool developed by the analogue circuit design group of the University of Dortmund. In co-operation with the University College London (ANSWERS, WP 2, Task 2.6) UNIDO-LBE will adapt fault tolerant circuit techniques to the resonant tunnelling LTGs as an architectural method to decrease the error probability of the investigated logic circuits. Together with the simulation results of TUE an extrapolation of the scalability of resonant tunnelling LTGs will be done.

Task 4.3 Planar RTD technology

A self-aligned GaAs-based planar resonant-tunnelling diode technology will be developed and characterised with respect to device tolerances. Ion implantation will be used for device isolation offering a more precise device mesa and hence device area definition. The impact of the ion implantation process on layer parameters will be taken into account. In particular, the manufacturability may be influenced by parameter changes like barrier thickness, interface quality, and doping concentration in the emitter region. The achieved data give a second source of data for a reverse engineering loop based on a more Si-compatible technology (WP 5).

Task 4.4 Industrial manufacturability analysis

The output from the experiments will be tested against our input models to try to achieve reverse engineering loop. This is the most critical part of the workpackage, and has never been achieved in the context of tunnel devices for analogue applications. If we succeed for digital circuits, a whole class of new device ideas become manufacturable. No matter how good a device performance, it may still not make it to the market place. A 'right-first-time' methodology, based on a sound reverse engineering capability, is essential for low-cost manufacture. This will be established as far as possible.

WP 4.1: Device level tolerance

The homogeneity and reproducibility of RTD devices was clearly demonstrated in task 2.1. The remaining problem is a precise definition of the device area. This aspect is further studied in WP 4.3. Using the standard InP-based technology we directly started to analyse circuits (WP 4.2). The functionality of the improved LOCOM MOBILE is based on a comparison of local device area. Hence, spatial as well as systematic variations of peak current density data are substantially

ruled out and a further improvement on the device level is of second order importance.

WP 4.2: Circuit level tolerance

E/D-type RTD-HFET devices and double-gate devices for non-inverting logic

Based on the technological improvement of fabricating enhancement and depletion type HFETs (E/D-HFETs) the circuit performance of the MOBILE gate is improved by using E-RTD-HFETs in the pull-down path of the input stage. The pull-up path of the MOBILE consists of D-RTD-HFETs to compensate the voltage drop of $V_{OUT}=V_P$ the output node during the monostable-bistable transition. Here, V_P is the peak voltage of the RTD. The combination of E/D type transistors is a key step to avoid performance degrading level shifting circuits and to enhance the voltage noise margins in multi-stage circuits when two inverting logic gates directly connected.

For a large scale integration of MOBILE circuits it is of fundamental relevance to improve the robustness of the basic logic gates and to estimate the impact of parameter variations on the circuit performance. Especially the pulsed power supply scheme of the original MOBILE, that is the simultaneous use of the supply voltage as clock was a significant drawback. Here, the critical point is that the logic voltage levels are determined by the amplitude of the supply voltage in the bistable state. Hence, it is very likely that the nominal logic voltage levels are affected by spatial as well as transient fluctuations of the supply voltage. If we consider the high-speed operation of MOBILE logic in the GHz domain, it is obvious that a separated power supply and high-frequency clocking scheme would improve the stability of the logic voltage levels.

A third important circuit modification is the replacement of the single clocking D-HFET by a distributed clocking scheme where each input RTD-HFET in the pull-up path has a double gate for the logic input and the clock signal. In connection with this modification it is also advantageous to use a single gate RTD-HFET for the pull-up device of the bistable RTD pair of the MOBILE which acts as a latch as soon as the devices in the input stage is switched off. The benefits of the distributed clocking scheme is a more area efficient layout and a greater flexibility of changing the logic circuit function because by adding or removing a double-gate RTD-HFET in the inputs stage the current driving capability is automatically adapted. In the former circuit configuration with a single clocking HFET the width of this transistor had to be carefully chosen depending on the fan-in. Altogether, SPICE simulations show that a MOBILE logic gate with double-gate RTD-HFET input stage and E/D type devices has a 30-50 % increased driving capability and enables shorter rising clock edges.

Robustness against power supply and clock voltage fluctuations

The usual way to control a MOBILE gate by means of a separate clock signal V_{CLK} is shown in fig. 4.1 for an inverter, where the clock signal is connected to the gate of an RTD-HFET [Prost 00]. This depletion-type RTD-HFET replaces the load RTD in the original MOBILE circuit. The circuit function is as follows: During the rising edge of the clock signal the output is connected to the power supply via the load RTD-HFET. Then, the monostable-bistable transition occurs and finally the gate switches to the desired logic state according to the input RTD-HFET. If the load RTD-HFET is switched of by $V_{CLK} < V_{th}$ the output is disconnected from the power supply and the gate returns to the rest state $V_{OUT} = 0.0$ V.

In fig. 4.1 two possible circuit configurations for a MOBILE circuit with dedicated clock input and constant supply voltage are shown. In fig. 4.1a the RTD is implemented on the source contact layer of the HFET. In the alternative configuration (fig. 4.1b) the RTD is placed on the drain contact layer of the HFET and is directly connected to the supply voltage. Connecting the

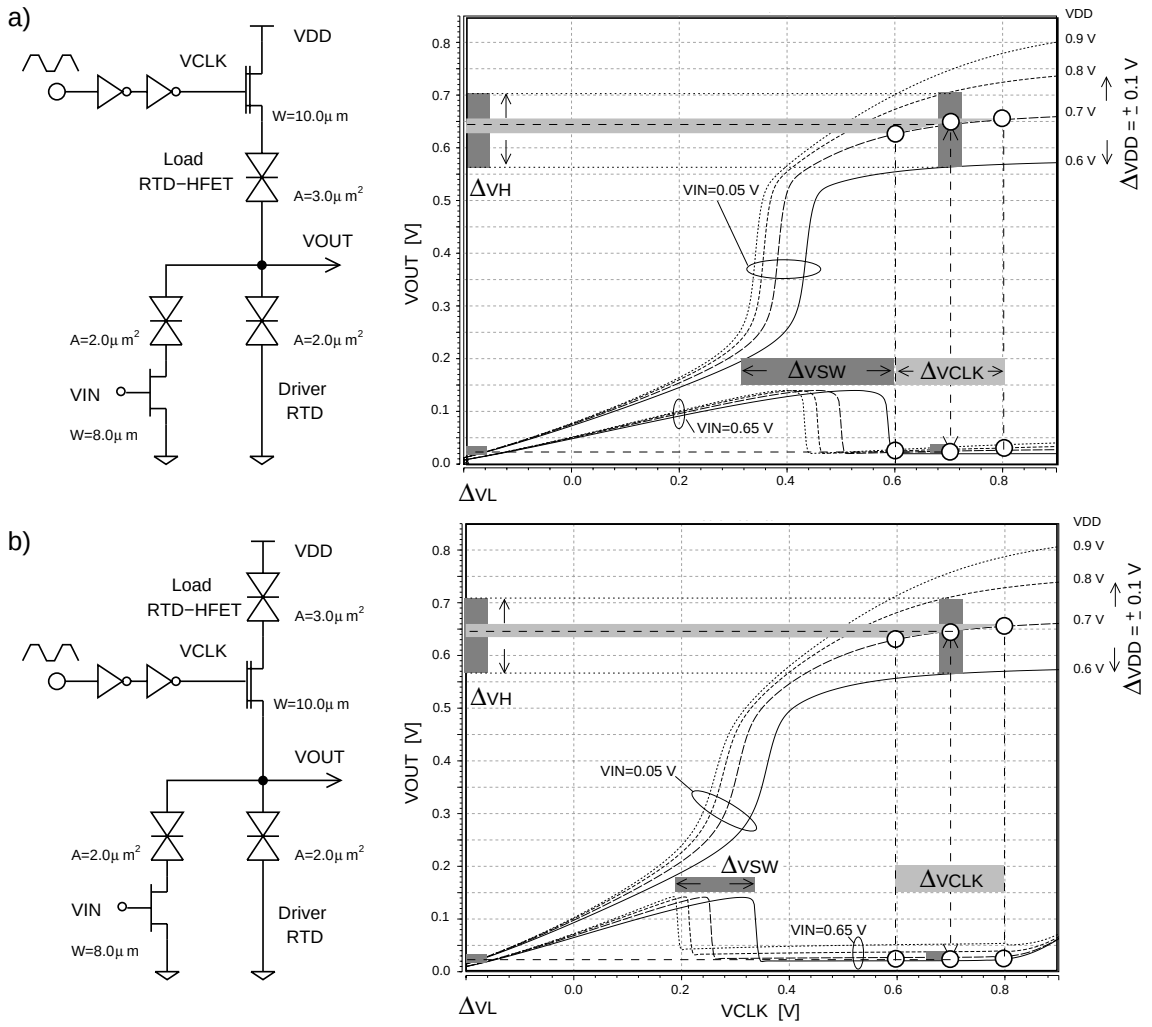


Fig. 4.1: MOBILE inverter with constant supply voltage and RTD-HFET as load element. The clock voltage is generated by an inverter chain using conventional E/D type HFET logic (DCFL or SBFL). Configuration (b) has the best driving capability and robustness of all investigated MOBILE circuit configurations because the clock RTD-HFET is operated with the maximum gate-overdrive and a voltage drop across the RTD as in (a) is avoided. The clock RTD-HFET in the pull-up path is a D-type device whereas the pull-down path is made of E-type RTD-HFET's.

HFET source to the output avoids the voltage drop across the RTD and thus the effective gate-source voltage $V_{GS} = V_{CLK} - V_{OUT}$ provides a larger gate overdrive. In both circuits the nominal supply voltage and clock amplitude are $V_{DD} = V_{CLK} = 0.7$ V for an RTD-HFET peak voltage of $V_P = 0.27$ V. The peak current density is $j_P = 21$ kA/cm2 and the minimum RTD-area of the input stage and the switching RTD D_2 is $A_{RTD} = 2$ µm2. The HFET gate has a length of $L_g = 300$ nm. The maximum transconductance is $g_m^{max} = 400$ mS/mm and $g_m^{max} = 350$ mS/mm for enhancement ($V_{t0} = 0.1$ V) and depletion type ($V_{t0} = -0.2$ V) devices, respectively. The are approximately the same as for the NAND/NOR gate, which was presented as a deliverable no. 2 in the 1998-1999 period of the project.

To evaluate robustness of the two MOBILE inverters against fluctuations ΔV_{CLK} and ΔV_{DD} of the clock signal V_{CLK} and the supply voltage V_{DD} the transfer characteristics V_{OUT} as a function of the clock voltage has been simulated for the logic inputs $V_{IN} = 0.03$ V and $V_{IN} = 0.64$ V. The supply voltage is varied between $V_{DD} = 0.6$-1.0 V in steps of 0.1 V. Since the logic transition of a

MOBILE is a highly non-linear and dynamic switching process the transfer characteristics is obtained from a transient SPICE simulation to consider the charging an discharging of the load capacitance. Here, a load capacitance of C_L= 30 fF corresponding to fan-out of 2 (FO2) and a clock slew rate of 1 V/ns have been chosen.

To estimate the deviation of the logic voltage levels from the nominal values V_L = 0.0215 V and V_H = 0.645 V an equal variation of ΔV_{CLK}= ΔV_{DD} = ± 0.1 V was assumed. Both variations affect the nominal logic voltage levels V_H and V_L in a different way. While the logic low level V_L remains nearly unchanged the logic high level V_H is affected to a greater extend. As indicated by the dark grey shaded areas the variation of V_H between 0.57 V < V_H < 0.72 V is primarily caused by the supply voltage variation. The voltage noise margin of V_H, defined as the difference between the minimal logic high voltage and the transition voltage V_{t2} of the RTD-HFET, where the output I-V characteristics is equal to RTD output I-V characteristics is

$$V_H^{NM} = V_H^{\min} - V_{t2} = 0.57\ \text{V} - 0.35\ \text{V} = 0.22\ \text{V}. \quad (1)$$

By choosing a slightly modified supply voltage of V_{DD}= 0.75-0.8 V this voltage noise margin can be increased. In general, the voltage noise margin of V_H is sufficient to avoid a logic fault, that is unintentionally switching off an RTD-HFET in the following logic stage. In contrast to this, the variation of V_L due to the clock voltage is less than 20 mV and thus the voltage noise margin

$$V_L^{NM} = V_{t2} - V_L^{\max} = 0.35\ \text{V} - 0.045\ \text{V} = 0.305\ \text{V}. \quad (2)$$

is slightly larger compared to the noise margin of V_H. Hence, it is very unlikely that an input RTD-HFET in the subsequent logic stage is switched on.

A critical point of the circuit in fig. 4.1a is that at very low supply voltages below V_{DD} = 0.6 V a simultaneous negative deviation of the clock voltage amplitude from the nominal value V_{CLK} = 0.7 V will prevent the gate from switching to the bistable state and thus leading to a logic failure. Simulations show that the switching point can be shifted to smaller voltages by increasing the HFET gate width but this also increases the clock load which has to be driven by the clock generation circuit. Consequently, an implementation of the RTD in the drain contact layer of the clock device (fig. 4.1b) offers a more robust circuit behaviour.

As far as voltage fluctuations are concerned, negative deviations of the supply voltage should be kept as small as possible to ensure a robust bistable state with a voltage swing of $\Delta V = V_H - V_L$ = 0.6 V. A somewhat unexpected result of this study is the negligible impact of the RTD peak voltage variation compared to the clock and supply voltage fluctuations. From the viewpoint of the technology the peak voltages were regarded as a critical device parameter because they are directly depending on the quantum well width. The reason for the overestimation of the impact of the peak voltage variations before analysing the impact of V_{CLK} and V_{DD} fluctuations was that any statistical deviation from the nominal layer stack would cause a strong shift the logic voltage levels. Nevertheless, based on the experimental data of the previous sections the assumed relative fluctuations of the clock and supply voltage $\Delta V_{CLK} / V_{CLK} = \Delta V_{DD} / V_{DD}$ = 14.3 % are much larger than the average deviation of the RTD peak voltage $\Delta V_P / V_P$ = 2-3 %. Even the 3σ peak voltage deviation of ± 24 mV from the nominal peak voltage V_P = 0.27 V does not show a significant shift of the logic voltage levels.

Trade-off between fan-in and peak current variation

Due to the current controlled switching mode we expect that any MOBILE circuit is highly sensitive to variations of RTD peak current, because the logic output state depends on the switching current I_{SW}, that is the difference of the current sums of the pull-down and pull-up devices at the output node. For simplicity we restrict our attention to an inverting logic where the

input RTD-HFETs are placed in the pull-down path. Then, the switching current for n inputs is

$$I_{SW} = I_{Load} - \sum_{i=1}^{n} I_{P,i} - I_{Driver} = \sum_{i=1}^{n+2} I_{P,i} \quad \text{for } I_{Load} = I_{P,n+1} \text{ and } -I_{Driver} = I_{P,n+1}. \tag{3}$$

In a MOBILE circuit with RTD-HFET input stage I_{SW} is a multiple of $I_P/2$ so that the switching current is always a quantised value and the logic output state is coded by the sign of the switching current. By choosing different areas for the load RTD and driver RTD the MOBILE gate switches to V_H if all inputs are off. In the compact implementation of this current comparator has been exploited in a threshold logic gate to reduce the circuit complexity of a full adder. Based on this example at least 4-5 inputs are required to obtain a sufficient functionality and performance [Pacha 00].

Referring to robustness of the MOBILE, the current controlled switching mode means that a strong deviation from the nominal peak current might change the sign of the switching current and thus causing a false logic output state. Since maximising the fan-in on the one hand and tolerating accumulated peak current variations on the other hand are contradictory objectives, there is a trade off between computational functionality and robustness. A simple first order approximation to calculate the maximum fan-in for a given peak current variation is based on the Gaussian law of error propagation. According to this approach, the mean deviation of the switching current increases proportional to the square root of total number of the devices n+2 of the MOBILE:

$$\sigma I_{SW} = \sqrt{\sum_{i=1}^{n+2} \left(\frac{\partial I_{SW}}{\partial I_{P,i}} \right)^2 \sigma^2 I_{P,i}} \quad \approx \quad \sigma I_P \sqrt{n+2} \qquad \text{for} \quad \left|\sigma I_{P,i}\right| = \left|\sigma I_P\right| = \text{const.} \tag{4}$$

To compute the correct logic output the absolute switching current variation has to be significantly smaller than the minimal switching current $I_P/2$ of the critical logic input combination:

$$\sqrt{n+2}\ \sigma I_P < I_{SW}^{\min} = \frac{I_P}{2} \tag{5}$$

From this follows the condition

$$2\left(\frac{\sigma I_P}{I_P} \right) \sqrt{n+2} \ < \ 1 \tag{6}$$

to compute maximum number of inputs for a given relative peak current variation. Assuming a typical 4-input gate, equation (6) is fulfilled for a peak current variation of $\sigma I_P/I_P = 5$ %. To include an additional design margin the 1σ-variation $\sigma I_P/I_P$ might be replaced by the 3σ-variation. In this case the maximum fan in would be approximately 5-6 input RTD-HFETs.

Worst case analysis for local peak current variation in opposite directions

In a more detailed worst case analysis it should be considered that a peak current variation will only cause a logic fault if strong deviations from the nominal value occur in opposite directions related to the position of the device in the pull-up and pull-down path of the MOBILE. Small variations will mostly affect the timing and can be treated similar to peak current variations in the same direction which are not a serious problem for the reliability of the circuit function. In addition, it is to expect that a multi-stage data path composed of random logic will always be influenced by the different fan-out and fan-in of the logic gates so that it is difficult to detect whether a delay or rise time variation is caused by the load capacitances or the variation of the device parameters. As soon as the total speed index, that is the ratio of the MOBILE switching current and load capacitance, is not reduced by an order of magnitude these timing variations are acceptable. This behaviour has been also confirmed by SPICE simulations where the delay and

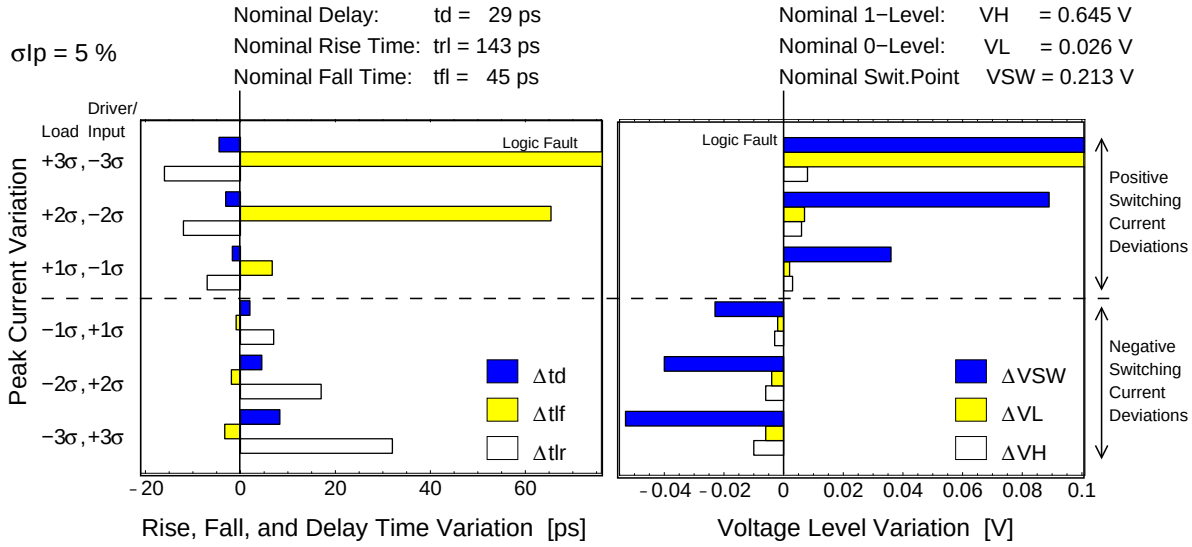


Fig.4.2: Time and voltage variations of a MOBILE inverter due to peak current variations of the load RTD-HFET and the pull-down path in opposite directions (worst case simulation).

rise time variations were negligible compared to the a fan-out loading factor of 30-40 ps/fan-out (FO1=15 fF), i.e. the increase of the output rise time per load capacitance.

Focussing on the peak current variations in opposite directions as the dominating error source a worst case simulation has been made. By changing the peak current according to {(+3σI_P,−3σI_P), (+2σI_P, −2σI_P),…, (-3σI_P, +3σI_P)} in the pull-up and pull-down path the impact of an absolute switching current deviation up to

$$\sigma I_{SW}^{\max} = 3\sigma I_P^{load} - \left(-3\sigma I_P^{driver} - 3\sigma I_P^{input}\right) = 9\,\sigma I_P \qquad (7)$$

is investigated. The circuit is specified for 1 GHz operation with a clock rise time of t_{CR} = 100 ps. As expected, an increasing peak current of the load RTD-HFET combined with a decreasing peak current of the input RTD-HFET and the driver RTD (σI_{SW}>0) reduces the output rise time for a logic low input V_{IN} = 0.03 V. For V_{IN} = 0.65 V a (+2σI_P,−2σI_P) variation corresponding to a switching current deviation of σI_{SW} = +6 σI_P leads to a temporarily metastable state so that the fall time t_{LF} = 110 ps of a logic low transition violates the timing conditions. If the variation is further increased to the 3σ-worst case (+3σI_P,−3σI_P) the total switching current variation of σI_{SW} = +9 σI_P causes a logic fault for V_{IN} = 0.65 V. Here, the current sum of the pull-down path is too small and the output makes a false logic high transition.

A negative switching current deviation σI_{SW}<0 caused by an increasing peak current of the pull-down devices simultaneously with a decreasing peak current of the load RTD-HFET reduces the fall time for V_{IN} = 0.65 V. The output rise time for V_{IN} = 0.05 V is affected in the opposite way, but here no logic fault can be detected even for the maximum –9 σI_P switching current variation. The detailed evaluation of the SPICE simulation is summarised in fig. 4.2. Overall, the deviations of the rise, fall, and delay times compared to the nominal specification are acceptable if the total switching current variation is less than σI_{SW} = 6σI_P.

Summarising the results of this study, the MOBILE logic gate is robust against supply voltage fluctuations up to ±0.1 V. The second important conclusion is that local peak current variations in opposite directions of the devices in the pull-up and pull-down path have the most critical impact on the error probability of the circuit. However, it is to expect that these special kind of local peak current variations are unlikely if the devices in a single gate are placed directly side by

side in an area of approximately 30µm×30µm. In this context more experimental studies are necessary to analyse the local and global parameter variations and their dependency on the minimum feature size.

WP 4.3: Planar RTD technology

This workpackage is dedicated to the development and the homogeneity analysis of a planar process for RTDs in the GaAs material system. The fabrication technology is based on ion implantation technique for device definition and isolation. A planar process has been established and fully functional ion implanted RTDs are presented. After the process has been optimised, a homogeneity analysis has been carried out. The results prove that the device tolerances are small enough for the application in digital logic circuits.

Process technology

The planar process consists of five process steps. In order to minimise the area and the series resistance of the collector contact, a combination of alloyed and non alloyed contacts has been chosen. Usually relatively large collector contacts are employed [Chen 97]. In contrast to that the layer structure on top of the double barrier quantum well in our process is thin enough to be able to alloy the ohmic collector contacts right through the double barrier. So the contact area can be reduced. As a consequence the emitter contacts have to be non alloyed contacts. This has also the advantage of a better manufacturability since alloyed contacts of small diameter are often problematic to reproduce.
In the first step the ohmic collector contacts are defined and alloyed deeply through the double barrier quantum well. The alloying process takes place at 480 °C for a period of 150 s in nitrogen atmosphere. SIMS measurements reveal that Ge atoms diffuse about 180 nm from the AuGe euthectic into the semiconductor material, so that they reach the highly doped collector layer.
Secondly the non-alloyed ohmic emitter contacts are defined. For the first samples an InGaAs layer with a graded indium content from 27% to 97% has been grown on top of the MBE layer stack. This has been replaced later on by a graded GaAs/InAs superlattice with a varying GaAs/InAs composition from 13/1 ML to 1/13 ML [Shiraishi94]. This greatly simplifies the epitaxy and thus contributes to a better reproducibility.
In the third process step the single devices are isolated against each other by means of a deep proton implantation. For that purpose they are covered with a 7 µm thick film of photoresist which can be structured by optical lithography and which is removed afterwards.
The devices themselves are defined by implantation with boron or oxygen ions in a self-aligned manner. The contact metallisation serves as the implantation mask. The implantation profile, i.e. the composition of ion energies, can be calculated with a Monte-Carlo simulator [Ziegler]. Experimentally it turned out that the exact energy profile as well as the ion dose needed for a sufficient isolation are not very critical parameters.
Finally interconnection lines and contact metallisation stripes can be evaporated in a fifth process step.

Experimental

The output characteristics of fully implanted samples exhibit a peak to valley ratio of about 4. The peak current densities are quite high and show values up to $6*10^4$ A/cm^{-2}. Besides the I-V characteristics are almost symmetric. The major drawback of these diodes are peak voltages of the order of 0.9 V, which is not ideal for digital applications. But there are ways to improve this behaviour: The layer structure has only been optimised with respect to a large peak to valley ratio in the GaAs/AlAs material system so far [Förster93, Förster94, Brugger91]. However, the conduction band profile of the double barrier structure can be altered in such a way that the

conduction band edge in the well is lowered in comparison to the undoped spacer regions. This can be reached by the addition of a small amount of indium to the well material. Thus the energy of the states in the quantum well is reduced and the onset of the first resonance decreases. An indium content of 8% suffices to cut back the peak voltage under 0.5 V. Yet this is accompanied by a reduction of the current density and the peak to valley ratio. So the right compromise has to be found for the use in logic units.

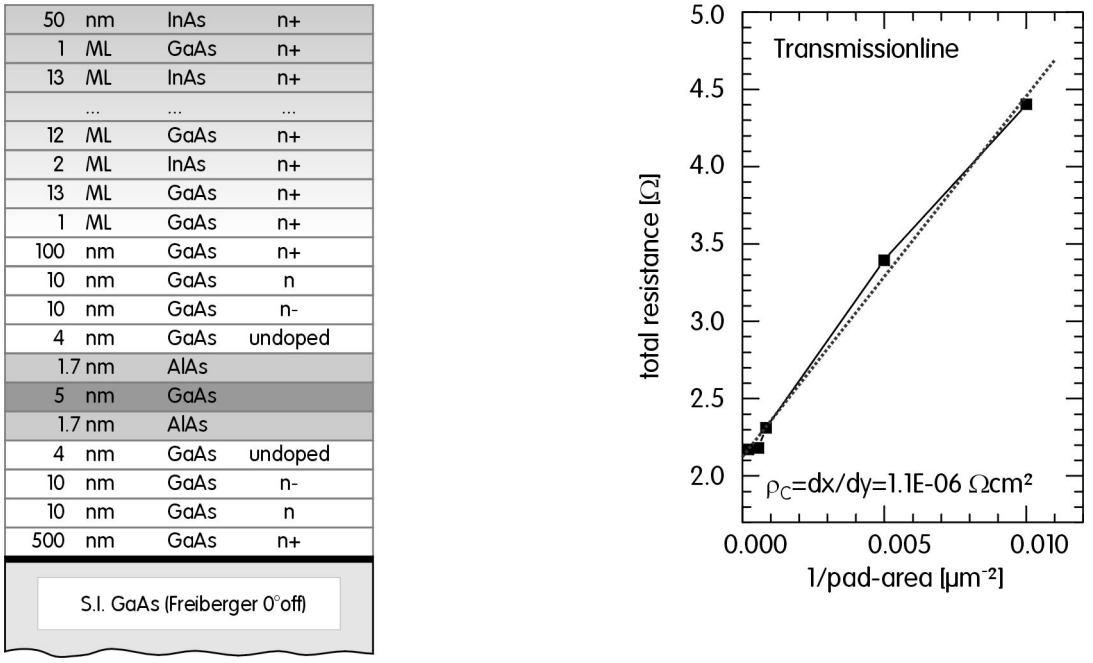


Fig. 4.3: MBE grown layer stack with an InAs/GaAs superlattice on top for the fabrication of non alloyed contacts. Transmissionline measurements reveal the good quality of the non alloyed contacts.

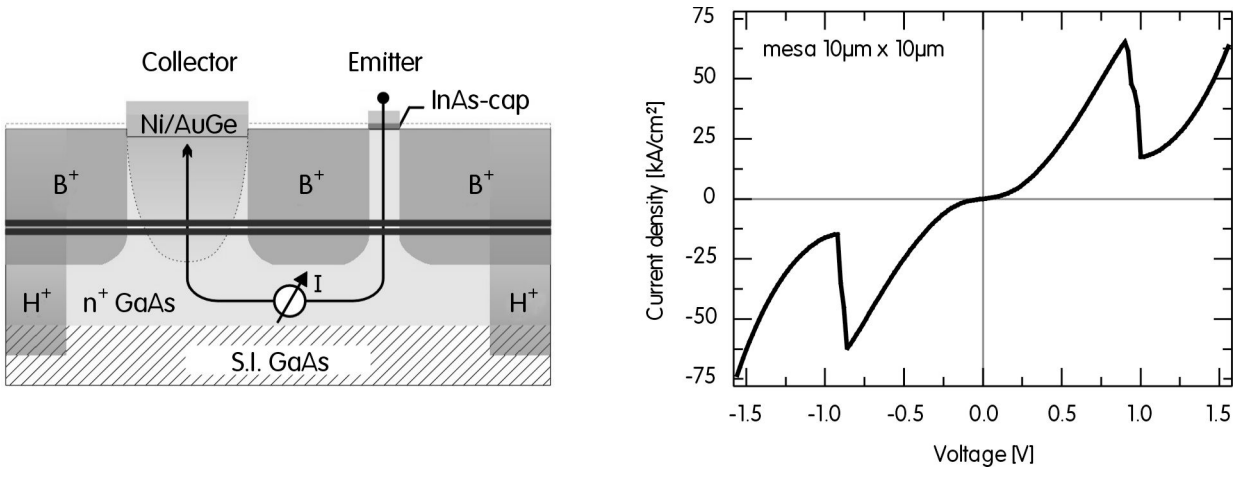


Fig. 4.4: A fully planar RTD with 6 ML thick barriers and without indium in the quantum well. The I-V characteristics is almost symmetric and exhibits a pronounced bistability in the NDR region for mesas of more than ~4 µm diameter.

Homogeneity analysis

A crucial point for the application of RTDs in digital logic circuits is the manufacturability of

those quantum devices. Points of special interest are the peak current density and the peak voltage of the I-V characteristics. For that purpose about 300 RTDs over a quarter of a 2 inch wafer have been measured and analysed statistically.
The variations in the peak current density are mainly determined by the homogeneity of the barrier thickness on the one hand and the spread in the device area on the other hand. The first can be attributed to the MBE growth procedure whereas the latter is caused by inhomogeneities of the device definition process. The question whether wet chemical etching or ion implantation is most suitable for this process is also addressed in this workpackage.

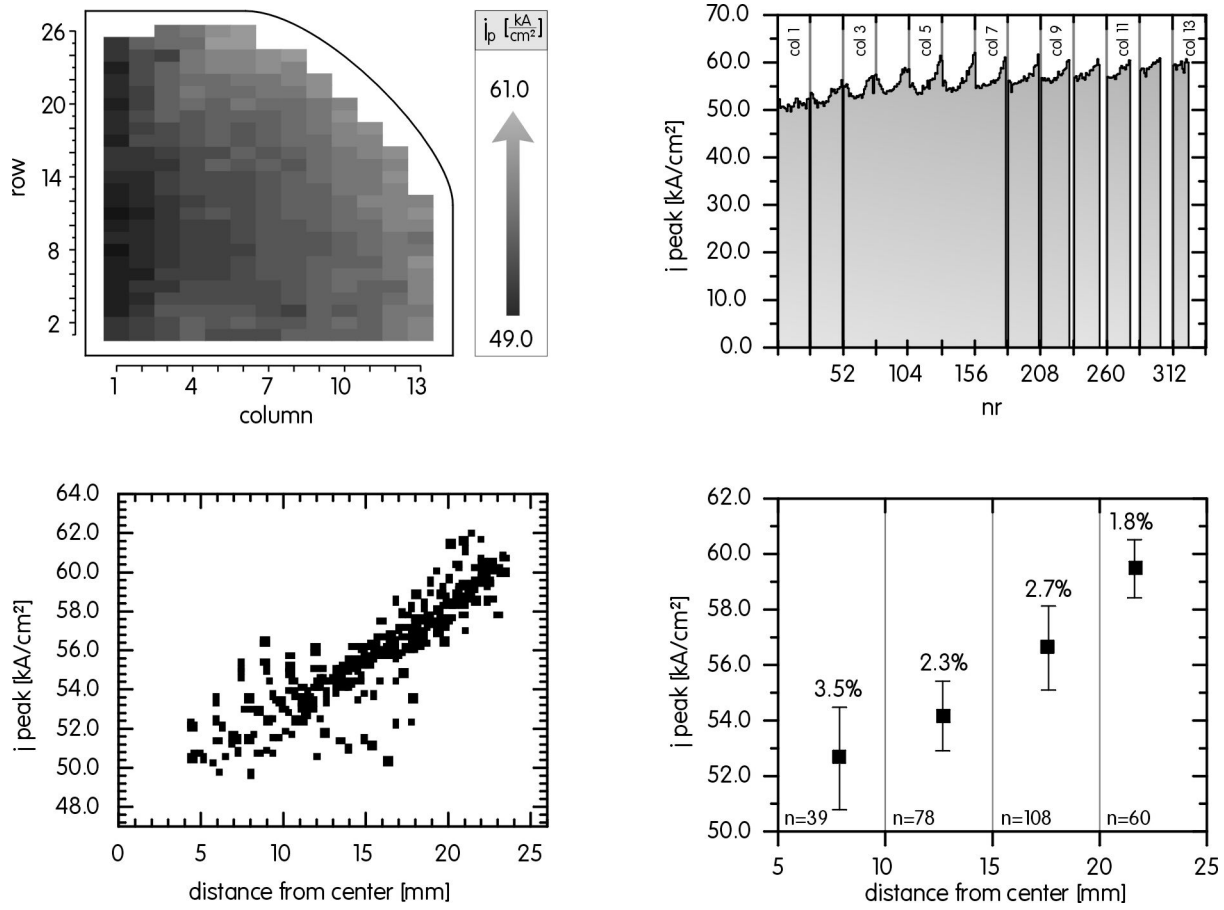


Fig. 4.5: Distribution of peak current density over a quarter of a 2 inch wafer. A radial shift in the peak current density can be seen which seems to be specific for MBE grown structures and which is system inherent. The overall homogeneity is 4.9%.

The RTDs under investigation have a device area of 49 µm² and exhibit a mean current density of (55.9 ± 2.73) kA/cm². This corresponds to an overall homogeneity of 4.9%. The grayscale plot as well as the scatter plot of the current density against the distance from the centre of the wafer reveal that there is a systematic shift to higher peak current densities towards the edge of the wafer. This phenomenon is MBE specific and has been reported in literature in the past [Billen97]. Possibly it is a consequence of the MBE cell geometry.
The distribution of the peak voltage shows a different behaviour. The mean value of the peak voltage for this series of diodes is (0.93 ± 0.04) V. This corresponds to an overall homogeneity of 4.3%. But the variations seem to be distributed more randomly over the wafer. The most probable contribution are inhomogeneities in the contact resistance which have a direct influence on the peak voltage. The assumption that the ohmic contacts need further improvement is supported by the fact that the peak voltage exhibits a clear dependence of the device area which

is typical for a substantial series resistance. This is not a general problem but a technological one and it can be solved. Furthermore there is the above mentioned possibility to reduce the peak voltage (together with the peak current density) by varying the layer composition in the quantum well.

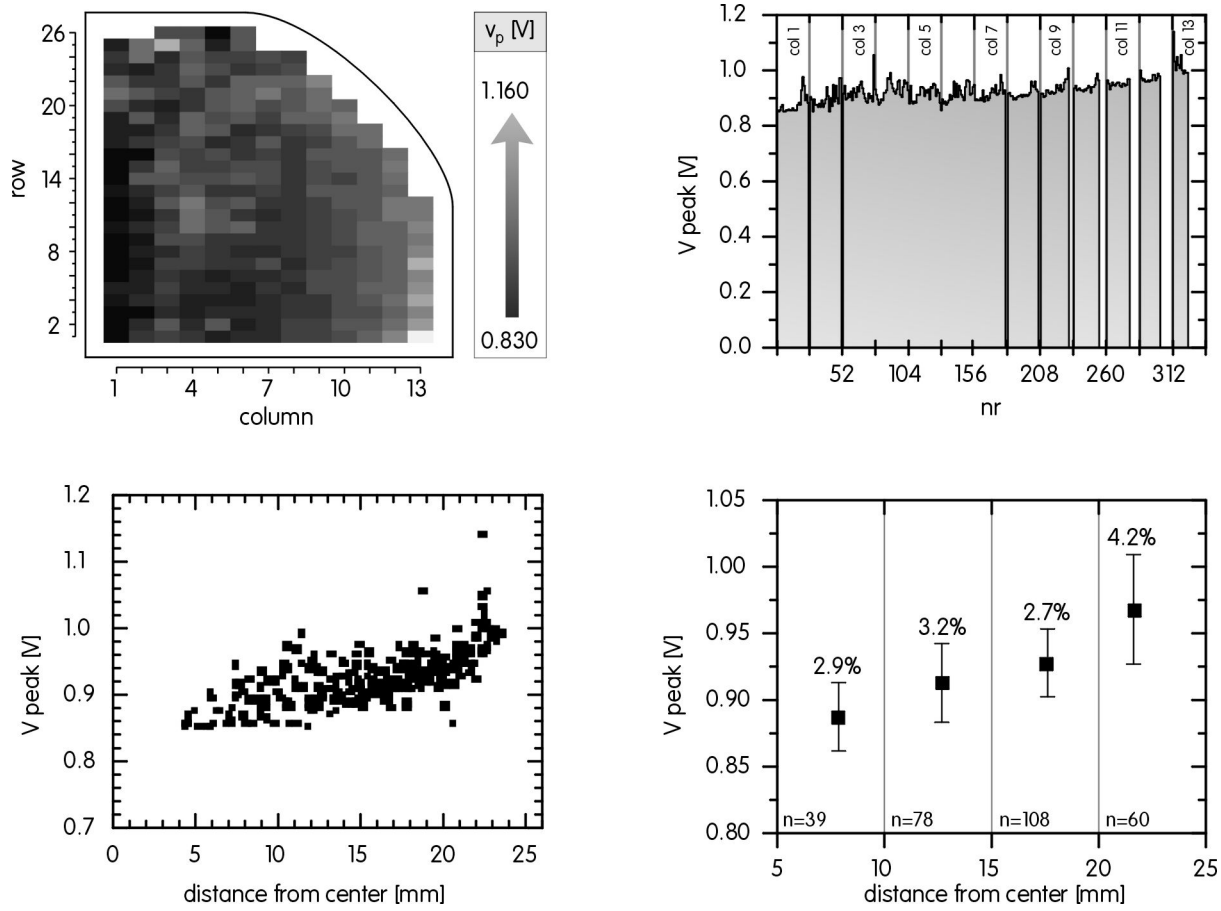


Fig. 4.6: Distribution of peak voltage over a quarter of a 2 inch wafer. The radial shift is less pronounced and the variations are more randomly distributed. The overall homogeneity is 4.3%.

Conclusion

A planar process for RTDs in the GaAs material system has been developed. The implanted devices meet the requirements in homogeneity for digital logic applications. Especially it should be stated that the MBE technique has developed to a state in which it offers sufficient control over the growth of those quantum structures.
Comparing the results of the etched and the implanted RTDs, both procedures provide a sufficient homogeneity. Considering that there are differences in the material systems and the technological facilities one can conclude that the etching and the implantation process yield comparable results as far as the quality of the diodes is concerned. The homogeneity of the peak current could be slightly improved by the planar process.

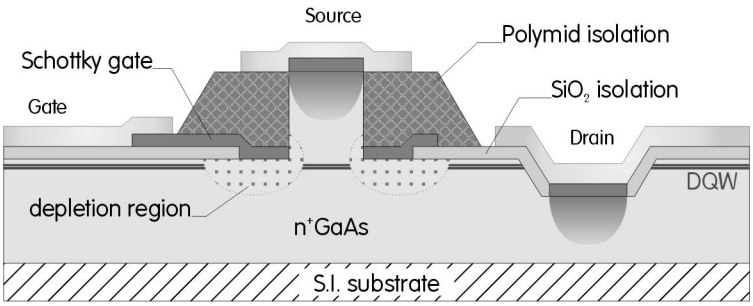
WP 4.3a: A vertical resonant tunnelling transistor (VRTT)

In this chapter extracurricular activities carried out at the Research Centre Jülich in connection with WP 4.3 are described.
One of the most important properties for the functionality of logic circuits is the

uniformity and reproducibility of the single semiconductor components like resonant tunnelling diodes or field effect transistors with regard to the influence of device deviations on the functionality of the logic circuit. The improved architecture for RTD/HFET gates that was developed within this project is so tolerant that the achieved homogeneity of the RTDs ensures a reliable operation of the logic unit. Still the concept of a vertical resonant tunnelling transistor could have some inherent advantages over the RTD/HFET integration as it should be less susceptible to spatial inhomogeneities during the epitaxy or the fabrication procedure.

Introduction

As has already been demonstrated in the past critical parameters for the safe operation of RTD based logic gates are especially the deviations in the peak current density and in the peak voltage of the resonant tunnelling diodes. Furthermore the integrated field effect transistors have to be designed in a narrow window of device properties with respect to the load or the drive RTD. Important parameters are here the transistor current with respect to the RTD peak current and the threshold voltage of the transistor with respect to the driving voltages in the logic unit. As could be shown in the project the improved design of a NAND circuit is very tolerant compared to other existing circuits in literature.



500nm	n^+GaAs	
200nm	n^-GaAs	
7nm	GaAs	spacer
1.7nm	AlAs	barrier
5nm	$In_{0.1}Ga_{0.9}As$	well
1.7nm	AlAs	barrier
7nm	GaAs	spacer
200nm	n^-GaAs	
500nm	n^+GaAs	
S.I. GaAs substrate		

Fig. 4.7: Scheme of a vertical resonant tunnelling transistor (left) and the corresponding layer structure (right).

From this point of view we paid attention to the manufacturability of the single RTD devices. The manufacturability could be improved by the development of a planar process for single RTDs. Although an improvement in the current density homogeneity could be achieved with this planar process systematic inhomogeneities lead to an enhancement of the growth rate at the wafer edge and can not be affected. In addition the reproducibility from one epitaxy to the other requires a high level of precision. It could be shown that all these points could be successfully fulfilled with a high accuracy. Nevertheless it could be a technological advantage to reach a higher level of tolerance and if possible to reduce the complexity of the devices.

Operation at room temperature

We have studied a vertical resonant tunnelling transistor which combines a single RTD with a vertical field effect transistor as an alternative approach. It could be shown in the past that this device has an excellent functionality at low temperatures [Förster98, Griebel98, Griebel99]. The I-V curve of the RTD could be tuned over a wide absolute current range. At voltages of about one volt the current channel could be depleted completely. Since low temperature applications in

logic circuits are not discussed seriously as an alternative in the framework of the project at present we extended the process for room temperature functionality. Fig. 4.7 depicts the examined layer structure and a principle scheme of the device layout of the resonant tunnelling transistor. The transistor is designed as a very small vertical mesa of a micrometer scale which is surrounded by a Schottky type depletion gate. By supplying a gate voltage with respect to the ground the effective cross section of the device can be changed and hence the absolute current can be set.

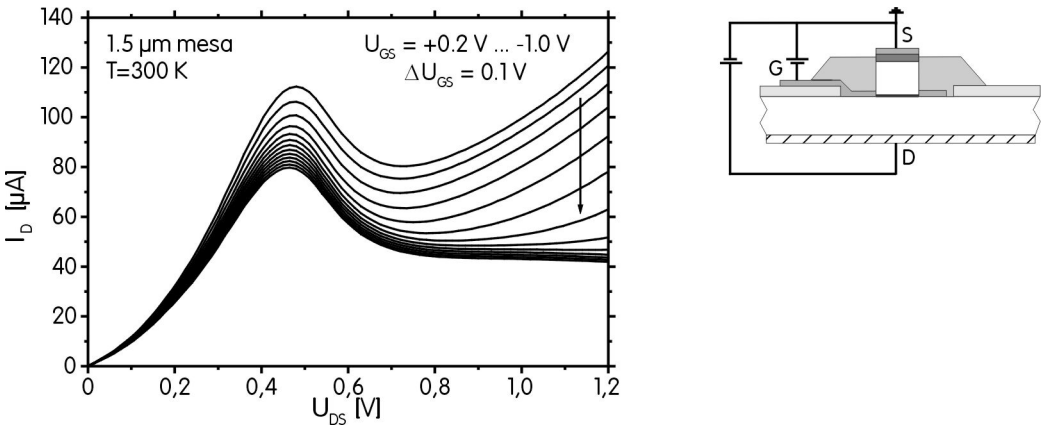


Fig. 4.8: I-V curves of a resonant tunnelling transistor measured at room temperature. The gate voltages have been varied between -1.0 V and +0.2 V.

Since there is an inherent coupling between the RTD and the transistor the adjustment of RTD parameters to transistor parameters is automatically fulfilled. An additional advantage of this design is that the mesa size can be processed very small and the complexity of the device can be reduced compared to RTD/transistor integrated circuits.
Fig. 4.8 demonstrates the room temperature functionality of the device. The peak current can be varied by 20% which is sufficient for MOBILE applications.

A VRTT-latch

The switching behaviour of the vertical resonant tunnelling transistors has been tested in a circuit of two VRTTs in series. In Fig. 4.9 the three dimensional bifurcation curve shows that the transition from the High to the Low state occurs very sharply at a few mV. This means that the current densities of two neighbouring diodes are very similar. It is also shown in the manufacturability study of single RTDs that there are very low deviations of devices that are close to each other. This is the most important point for the MOBILE functionality. As could be shown from PSpice simulations the bifurcation diagram is not strongly affected by variations in the absolute values of current densities. The most important parameter is the span between the load and the drive current density. The functionality will not be strongly affected if the absolute value of the diodes differs over the wafer or from one wafer to another.
The circuit in Fig. 4.9 was also used to demonstrate the low frequency switching functionality. The output signal is shown as a function of the input and the clock voltage. This kind of circuit acts as an inverter unit and demonstrates the self latching operation in the output signal. The clock voltage pulses were 1.2 V, the gate voltage was switched between -0.2 V and +0.2 V [Stock01].

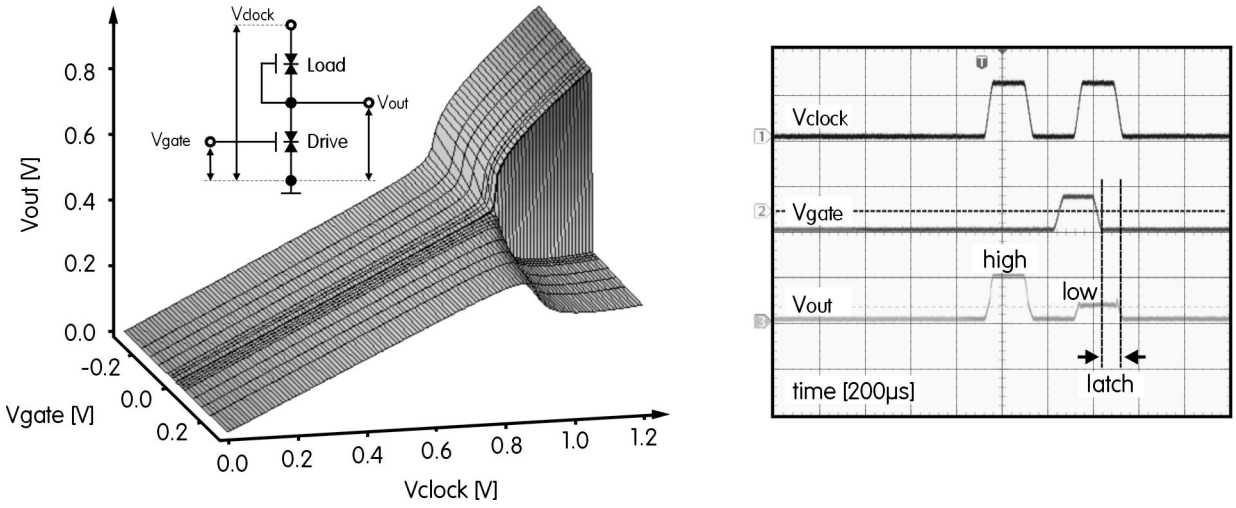


Fig. 4.9: Low frequency self latching inverter build up with two vertical resonant tunnelling transistors. The three dimensional plot of the bifurcation curve and a scheme of the circuit are shown on the left.

Conclusion

In conclusion it could be shown that the vertical resonant tunnelling transistor operates at room temperature and has some serious advantages over the RTD/HFET integration. The demands on the matching between RTD and HFET are inherently fulfilled and this concept offers the potential for reaching a reduced complexity.

WP 4.4: Industrial manufacturability analysis

At the beginning of the LOCOM project the impact of epitaxial growth in the nm-scale was dramatically overestimated. Meanwhile it is clear that the modern growth methods like MBE clearly fulfils circuit requirements. The mayor problem is the precision of device area definition which is a standard problem of micro- and nano-fabrication. The industrial manufacturability has been analysed in terms of

(1) technology

(2) reverse-engineering

(3) transferability to production

This report is provided by M J Kelly, University of Surrey, Guildford, UK as a subcontract to the Gerhard Mercator University of Duisburg. The subject matter is a review of the manufacturability of tunnel devices, and complements experimental work undertaken at the University of Duisburg, and reported in the first annual report.

Technology

The LOCOM project takes as its starting point the existence of a wide range of semiconductor devices (transistors used in logic and memory devices, lasers in communication systems and many microwave components) that employ the phenomenon of quantum mechanical tunnel through thin layers of wide band-gap III-V semiconductors. These devices achieve superior performance (speed, low power consumption, low noise, low sensitivity to temperature, light efficiency, high sensitivity detection etc) by exploiting the tunnelling current [Wilkinson et al., 1997]. Within LOCOM a number of hybrid devices, based on combinations of resonant

tunnelling double-barrier diodes and heterojunction field-effect transistors, have been demonstrated as the MOBILE device for high-performance NAND/NOR operation.
Almost all research undertaken on tunnel devices before the start of LOCOM have been based on the proof of principle, where the existence of high performance devices functions were demonstrated, usually on a one-off basis. Besides the superior performance, such manufacturability studies should include high yield, reproducibility, reliability, a capability for reverse engineering, a right-first-time design process, and design tolerance, all of which translate into low cost per unit device. If the superior device misses any of these attributes, the chance for production drops rapidly.
The reason for slow progress on manufacturability of tunnel devices is very simple: the tunnelling process that determines the current flow through a given tunnel barrier is exponentially sensitive to the thickness of the barrier and to its height. For typical layers in the GaAs/AlAs system for example, a one monolayer variation on a single tunnel barrier layer that is supposed to be ten monolayers thick results in a ±360% variation on the desired current density [Wilkinson et al., 1997]. (This results is achieved with a simple simulation.) For the designers of microwave systems, and more generally for digital or analogue applications, such variations are intolerable, with a figure closer to ±20% being the tolerable upper limit. Such a variation is consistent with devices being accurate to approximately ±0.1 monolayer, and growth studies have not achieved this lever of control that is required both as uniformity across a wafer and wafer-to-wafer reproducibility. The physics associated with resonant tunnelling makes some modifications to the ±360% figure above, reducing it to more like ±100%, but even this places very strict limits on what can be tolerated.

Progress at Surrey 1988-2000

Throughout LOCOM there has been a major programme at the University of Surrey concentrating on the manufacturability of single-barrier tunnel diodes for microwave applications [Syme 1993] that place the much tighter demands on materials growth and assessment than is required for the main programme. This Surrey programme has been funded in small part by LOCOM but mainly by the UK's Engineering and Physical Sciences Research Council under contract GR/N27791 due to be completed on 28/02/2001.
The first part of the project consisted on a detailed study on the statistical variability in device performance that could be expected based of fluctuations in the layer thickness and the length scale of lateral variations in the thickness of the tunnel barrier across the wafer. These results reinforced the need for achieving accuracy to ±0.08nm of about 0.3 monolayers to achieve acceptable uniformity and reproducibility of device characteristics [Kelly 2000].
The second part of the study was the repeat of an earlier, failed, exercise to establish manufacturability [Wilkinson et al., 1997] of the single-barrier diode, the so-called ASPAT diode (asymmetric spacer layer tunnel diode). The first exercise used commercial suppliers both of epitaxially grown material and of materials qualifications, and a simple simulation package. The first exercise failed, as the commercial growers had never tried to achieve the level of accuracy now required, and the various methods of materials characterisation used to established that the grown epitaxial multilayers were as specified just did not have sufficient accuracy or precision. Transmission electron microscopy could handle the barrier layer, but not to sufficient accuracy without detailed and time-consuming modelling of diffraction patterns. Furthermore the technique is destructive. Ideally what is needed is an accurate, precise, non-destructive technique that can easily be deployed to map the uniformity across wafers.
The repeat exercise has been carried out with a research molecular beam epitaxy (MBE) machine, and has involved a form of rapid ex-situ characterisation of one sacrificial wafer grown daily that can be followed in a production environment by up to 20 wafers grown to specification, this reducing yield and raising costs by only 5%. The process involves growing a

structure that combines a relatively coarse-scale calibration structure consisting of an GaAs/AlAs superlattice and a doping staircase that can be examined by X-ray crystallography and C-V profiling to get the growth rates of the materials and the accuracy of the doping profile within two hours of growth. The results from such a test wafer can be used to fine tune the MBE growth conditions to hit the target figures more precisely. This exercise has been used to grow one wafer of a single-barrier diode structure each month over three months (each using a new calibration layer), repeated twice with refinements to the calibration layer in between [Hayden et al. 2000, Hayden et al. submitted]. The rms spread in device characteristics achieved from six different wafers and different process runs has been 8, 11, 9, 10, 6, 9, 2, 8, 17%. This last value has a systematic variation across the wafer, without which the figure is lower than 10%. An rms deviation of 6% would give a 3-sigma variation of ±20% variation needed by systems designers. It is clear that we are near to achieving this. The wafer-to-wafer reproducibility of the later set of wafers is very good for two wafers (±3%), but a third is still off by 25%, and work is still in progress to eliminate this. The data is shown in Tables 1 and 2, as a collection of the average current density of diodes of different areas for a fixed 0.4V forward bias, and in Figure 1, as a graph shown the current density as a function of radial position on the wafer for the six diodes.

Progress Elsewhere

The earliest work on reproducibility of tunnel devices concentrated on the double barrier diode in the AlAs/GaAs system [Mars et al. 1993], recording a standard deviation of 10% in the peak current density within a wafer and a 20% variation on the average from wafer to wafer. Within the LOCOM project, work at Duisburg has concentrated on the InGaAs/AlAs system, and has demonstrated a variation of 4.7% in peak current density within wafers and a 9.1% variation between wafers [Prost et al. 2000] and work on AlGaAs/GaAs has been carried out in Jülich resulting in homogeneity of better than 5 % for both peak-current and peak-voltage homogeneity [Förster 2000]. LOCOM indicates a reproducibility that is adequate for the applications in digital systems where a clock pulse can be used to reset binary voltage levels.

Future Work on Manufacturability

Of the list of characteristics for low-cost manufacturability, we have established the superior performance of the ASPAT diode (the device has a wide dynamic range as a detector, very low sideband noise, and a very low sensitivity to ambient temperatures. We know that the devices are reliable, and we have now shown that that can be made reproducibly to a high yield. We know that the design is not tolerant to small variations in parameters, but we have shown that the ex-situ growth calibration technique can be used to overcome this lack of tolerance. Only two features are left, the reverse engineering and the right-first-time design capability. Both of these will require simple modifications to the simulation tool, making it capable of handling series resistances and capable of giving barrier parameters based on measured I-V data. This will be the focus of a future research programme. For double and multiple barrier resonant tunnelling devices, there is a wider range of transistor, laser and microwave applications, the transistor applications of which are being explored in LOCOM.

With epitaxial wafers being quoted at $1500 each and with processing costs to match, the cost of microwave diodes are about 30¢ from a 2" wafer and 15¢ from a 3" wafer. With adequate uniformity and reproducibility, such diodes with their superior performance then become very competitive elements in hybrid systems, e.g. automotive radar applications. The digital circuit applications have costs associated with circuit area, but the resonant tunnelling growth does not add appreciably to the cost over that of a single heterojunction wafer, in spite of the greatly superior performance that MOBILE and other circuits based on resonant tunnelling will deliver.

Manufacturability of Tunnel Devices

Over the period of LOCOM, the new results have shown that the tight tolerances required of materials growth to produce devices with a narrow spread in their electrical properties is now possible. The results apply to both single barrier and double barrier structures in GaAs/AlAs and InGaAs/GaAs. Until now, this step had never been established satisfactorily. This is a major advance, enough on its own to justify much of the LOCOM budget. With all the extra results on circuit performance the whole project has been a very important step on the way to the realisation of commercial tunnelling devices and circuits.

Table 4.1 : The doping of the top and bottom contacts, as measured by secondary ion mass spectrometry and C-V profiling. Although close reproducibility is established, the systematic difference between that specified and that measured is an important ingredient in the next task of achieving a right-first-time design.

		Speci-fication	A	B	C	D	E	F
Top (10^{18} cm^{-3})	SIMS		3.6 ± 0.1	4.0 ± 0.1	3.65 ± 0.13	4.84 ± 0.2	4.76 ± 0.2	4.79 ± 0.2
	CV	3×10^{18}	2.76 ± 0.02	3.14 ± 0.02	3.10 ± 0.05	4.24 ± 0.02	4.24 ± 0.02	4.04 ± 0.03
Base (10^{18} cm^{-3})	SIMS		3.72 ± 0.09	4.00 ± 0.09	3.77 ± 0.12	4.92 ± 0.2	4.83 ± 0.2	4.93 ± 0.2
	CV	3×10^{18}	3.02 ± 0.04	3.18 ± 0.04	3.20 ± 0.05	4.06 ± 0.03	4.12 ± 0.03	3.95 ± 0.04

Table 4.2: The electrical statistics (average current densities at 0.4 V forward bias, and the rms deviation values expressed as a percentage of the average) obtained from devices of two different areas from six different wafers.

Wafer	A	A	A	B	B	B	C	D	D*	E	F
Area (10^3 µm²)	10	27.5	All	10	27.5	all	27.5	10	10	10	10
Average (A/cm²)	237	160	201	275	222	251	199	160	167	123	129
Std. Dev. (%)	8	11	21	9	10	14	6	9	2	8	17

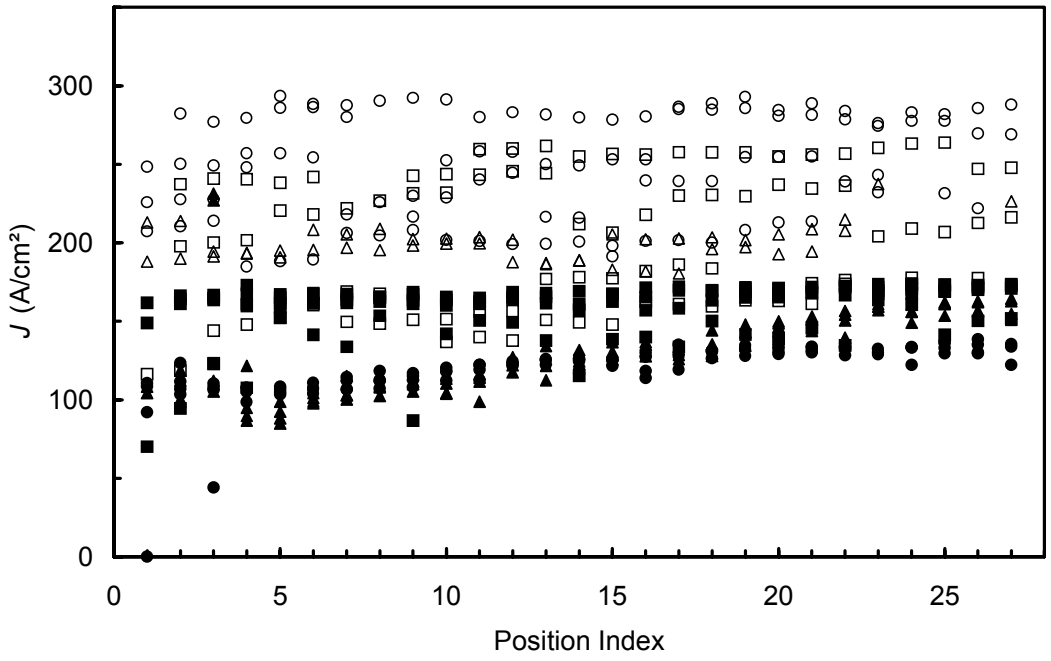


Fig.4.10: The measured current densities at 0.4V forward bias as a function of the position on the wafer, with devices from wafers A( ), B(o), C(Δ), D( ), E(o) and F(Δ).

Reverse-Engineering

From the very beginning LOCOM settled up a mature modelling activity in terms of both

- physical device simulation, and
- SPICE circuit simulation.

These activities are tested against experimental results. The physical simulation proved that the sensitivity data of I-V-parameters against technological fluctuations is within the realisable homogeneity and reproducibility [Prost 00]. The SPICE software is based on device models obtained from experimental results. These models allow to design and to model the predicted performance of any logic circuit. The available platform of models, however, is restricted to logic circuits and has to be extended in order to predict precisely memory or analogue RTD-based circuits.

Transferability to production

This aspect is the most critical one because it is affected by all manufacturability issues. The most important is the absolute need of the LOCOM approach to reach certain performances and markets which are not achievable with competing but existing approaches. Suggested that the final LOCOM demonstrator "Full Adder" is available the following possible applications were explored within the last year:

- high speed numeric applications
- hearing-aid manufacture

The Full Adder is the basic computing element for any numeric operation and may replace together with simple shift operations nearly all mathematical functions. Prof. Goetze from the University of Dortmund, Institute of Informatics, is working on this subject and presented a

seminar to the LOCOM partners discussing this aspect. We agreed to further explore the possible application of the Full Adder after availability for this purpose.

A direct path to manufacture has been explored in a visit at Siemens, Hearing-Aid Production, in Erlangen, in December 1999. Dr. Holube (Siemens) and Dr. Prost discussed the possible application of LOCOM circuits with following results:

The low supply voltage is clearly below the lowest available CMOS technology (> 1 V at reduced speed data, standard > 1.3 V). The provided high speed is of interest for improved digital signal processing. However, the available VLSI CMOS technology allows a massive parallel processing of data at reduced speed and with overall lower power consumption.

WP 5: Transfer to Silicon

Task 5.1 Experimental study on novel Si-based NDR devices (UNIDO, SiQUIC, Daimler Benz)

Based on the device simulations on Si-NDR devices (TUE, WP 5.1), UNIDO will design and simulate an LTG-circuit by combining Si-based NDR devices and MOSFETs. In an reverse engineering loop TUE will modify and simulate the devices to include the investigations from the circuit level simulations. The Daimler Benz Si-Ge group at Ulm, headed by Dr. U. König and the SiQUIC consortium will deliver layer stacks for Si-based NDR-devices. Further processing steps (etching and contacting) will be done by the technology group of UNIDO who will also perform test and measurements.

Task 5.2 Exchange with Si-technology within MEL-ARI (SiQUIC) All LOCOM Partners)

A common meeting of the SiQUIC and LOCOM partners will be organised to merge the results of both projects in the direction of preliminary Si-NDR devices. The results of the TUE devices simulations on Si-Esaki tunnelling diodes and Si-Ge RTDs will be transmitted to the Daimler Benz research group at Ulm and to the MEL-ARI SiQUIC consortium.

WP 5.1: Experimental study on novel Si-based NDR devices (UNIDO, SiQUIC, Daimler Benz)

This workpackage aims at the experimental study on novel Si-based NDR-devices regarding a transfer of the LOCOM-concept to Si-technology. In principle, there are two different types of tunnelling structures exhibiting NDR: Resonant tunnelling diodes (RTD) based on double barrier quantum wells [Ismail91] and Esaki interband tunnelling diodes (ITD) exploiting the band bending at a p^+/n^+ junction [Duschl00]. The performance of state of the art Si/SiGe RTDs, however, is strictly limited by their intrinsic properties. In particular, large effective masses and relatively low barrier heights in Si/SiGe heterostructures causes peak-to-valley ratios (PVR) which are not much larger than one at room temperature [Ismail91] - not sufficient for circuit applications based on LTGs. On the other hand, state of the art ITDs exhibit PVR of more than five at reasonable current densities of 8 kA/cm² [Duschl00].

Within the scope of LOCOM Si-based ITDs have been developed which are expected to be well suited for digital applications. The epitaxial layer structures are provided by the Max-Plank-Institute Stuttgart. The processing is performed at the GMUD using a novel one-metal ITD-design. A latch is build up showing a similarly bifurcation curve as InP-based RTDs. Since low power MOS-FET or SiGe-HFET are available which are expected to be able to be monolithically integrated with such ITDs, Si-based high performance logical circuits based on the MOBILE-concept should be principally manufacturable.

Growth and fabrication of SiGe-ITDs and demonstration of a SiGe-MOBILE

Two different Si-Ge-ITDs are investigated. The first structure (S1393) consists of a 50 nm thick B-doped Si p^+ (5×10^{19} cm^{-3}) buffer layer, followed by a *p*-type δ-doping layer (1×10^{14} cm^{-2}), a $Si_{1-x}Ge_x$/1 nm Si intrinsic zone, a *n*-type doping layer (1×10^{14} cm^{-2}), and a 100 nm thick P-doped Si n^+ (5×10^{19} cm^{-3}) cap layer (cf. Fig. 5.1, left).

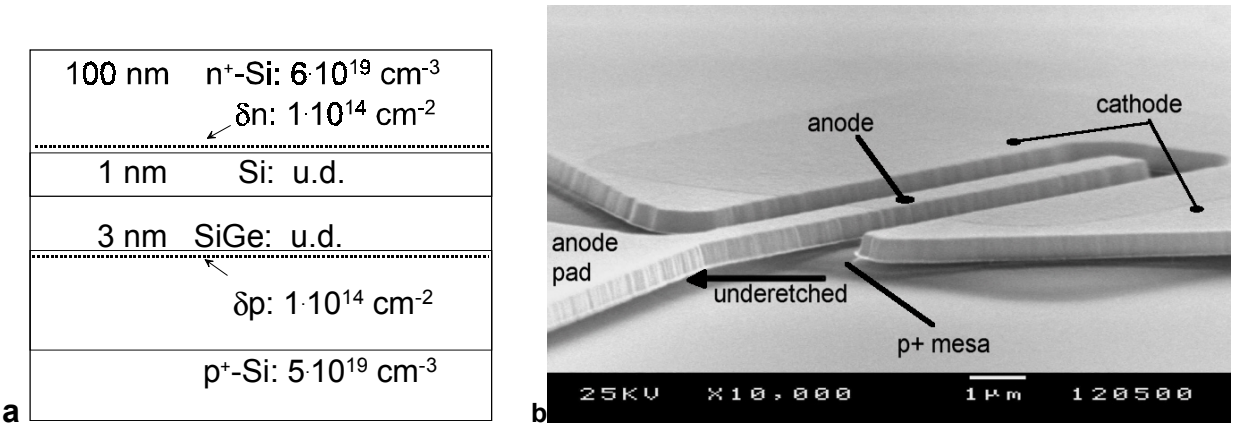


Fig. 5.1: Si/SiGe Esaki diode grown by R. Duschl, MPI Stuttgart: (a) Epitaxial layer structure and (b) device layout.

In type S1408 the thickness of the highly p-doped buffer layer was extended to 280 nm to facilitate the processing. The layer structures were optimised regarding the peak current density (PCD) and the peak-to-valley ratio (PVR) resulting in a Ge-content of 48% while 3 nm is at the upper limit for the pseudomorphic growth of $Si_{0.52}Ge_{0.48}$. The position of the SiGe layer within the *i*-zone was found to be crucial for the tunnelling probability and therefore for the I–V characteristic. Growing the SiGe layer directly at the δP layer without any Si spacer layer deteriorates the device performance, whereas the growth of the SiGe layer directly at the δB layer reduces the B diffusion and supports the transfer of the holes into the SiGe layer. Both effects increase the tunnelling probability.

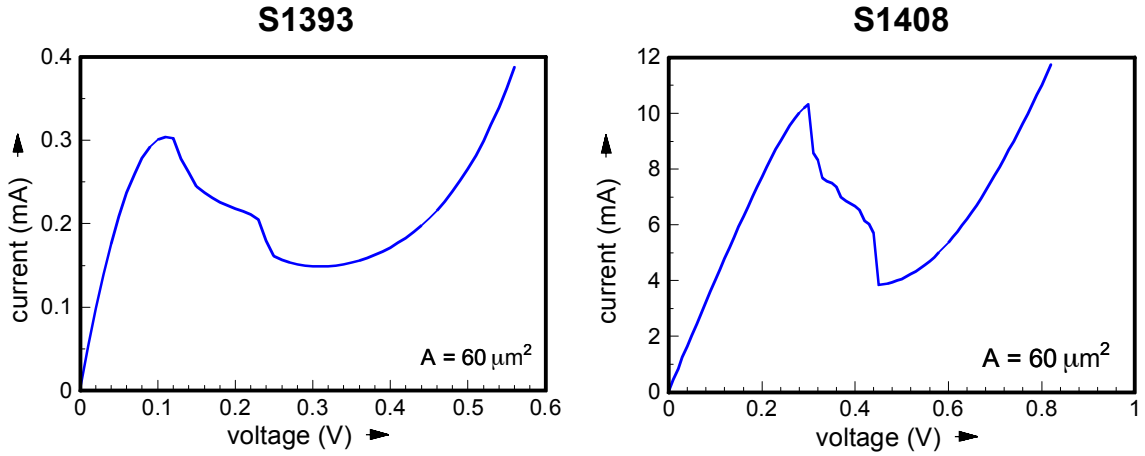


Fig. 5.2: Measured I-V characteristics of the 1-metal ITD in forward direction.

The fabrication of the 1-metal ITD starts with the removal of the natural oxide layer in HF(1%). After the evaporation of Ti/Pt/Au (30 nm/30 nm/340 nm) serving simultaneously as the anode and cathode metal contact (cf. Fig 5.1, right), the structure was etched down to the p^+-buffer in order to isolate anode and cathode. For this purpose KOH (10%, 40°C) is well suited because of its high selectivity to n- and p-doped material. A final etch step using HNO_3:HF (98:2) removes the p-doped buffer and isolates the contact pads by under etching the anode-interconnection finger. Fig. 5.2 shows the I-V-characteristics of the two types of ITD exhibiting an anode area of 60 µm².

The sample S1393 shows a peak voltage V_{Peak} of 110 mV, a peak current density of J_{Peak} = 0.52 kA/cm² and a PVR of 2,1 while sample S1408 exhibits V_{Peak} = 296 mV, J_{Peak} = 17.1 kA/cm² and

PVR = 2.6. Except the PVR, the I-V characteristic of S1408 is similar to that of the InP-based RTDs designed for the LOCOM-project.

Both types are well suited for logical circuits based on the MOBILE concept as demonstrated in Fig. 5.3 showing the bifurcation curve of the ITD-latches. The bifurcation curve is obtained by applying a voltage V_{clk} over two serial connected ITDs (forming the latch) and measuring the output voltage for different input currents I_{in} into the common node (MOBILE concept). Remarkable is the very low power consumption per unit area of sample S1393. At a clock voltage of V_{clk} of 400 (600) mV, the low and the high level are V_L = 32 (79) mV and V_H = 363 (521) mV, respectively, resulting in an almost perfect voltage swing $\Delta V = V_H - V_L$ of 83 (87) % of the applied clock voltage. The type S1408 exhibits a bifurcation curve typical for an InP-based RTD-latch. The characteristic voltages are V_L = 104 mV and V_H = 582 at V_{clk} = 700 mV.

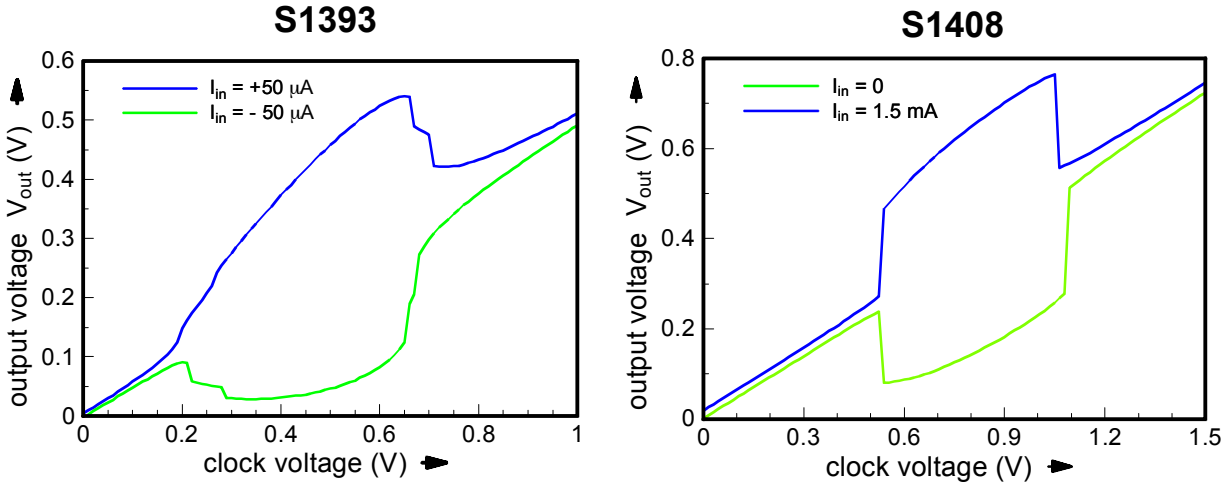


Fig. 5.3: Bifurcation curve of the ITD demonstrating the MOBILE functionality in the Si-based material system.

Speed of SiGe-ITDs in comparison to InP-based RTDs

Using a HP8510C network analyser, the high frequency performance of the SiGe-ITDs have been measured from 45 MHz to 45 GHz and compared to results obtained with LOCOM-based RTDs at the same layout ($A = 3\times20$ µm²).

In order to estimate the maximum oscillation frequency, the small signal elements of a equivalent circuit model of the ITDs (inlet in Fig. 5.4) have been extracted using an optimisation algorithm based on the simulated evolution [Goldberg89]. Fig. 5.4 shows the bias dependent parallel capacitance C_P and conductance g_P forming the intrinsic ITD. The extra-inserted R-C-branch models the finite specific resistance of the Si-substrate.

Due to the low current density of S1393, all S-parameters versus frequency are smooth resulting in a good agreement between measured and modelled data even in the NDR-regime. The extracted conductivity corresponds to the DC-data $g_P = dI/dV$.

In the NDR-regime of the high current density ITD S1408, the measurement set-up could not be stabilised at low frequencies. Therefore the extracted data in this regime have to be interpreted very carefully. However, the higher conductance in combination with the higher capacitance results in the same maximum frequency as of S1393 (fig. 5.5). In comparison with an InP-based RTD with the same device layout, the SiGe-ITDs are about 15× slower. This is due to the high capacitances caused by the very thin undoped layers between the δ-dopings.

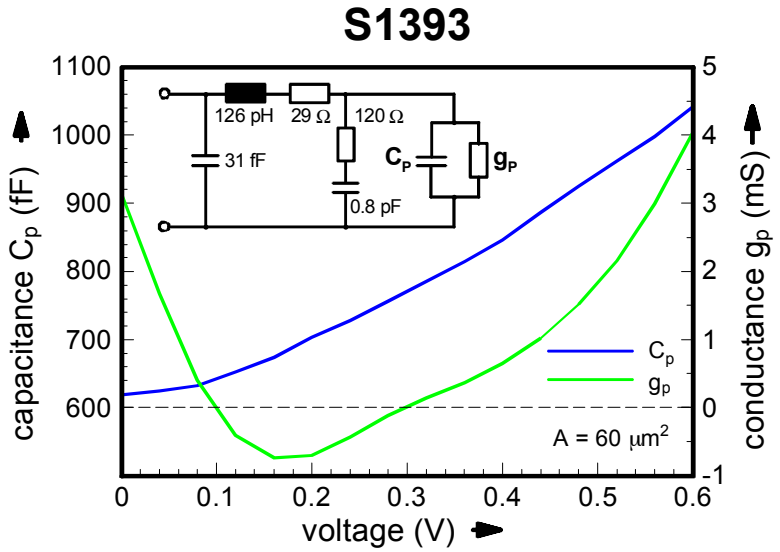


Fig. 5.4: Small-signal equivalent circuit of the ITD and the voltage dependent ITD-capacitance and conductance extracted from the best fit to the measured S-parameter.

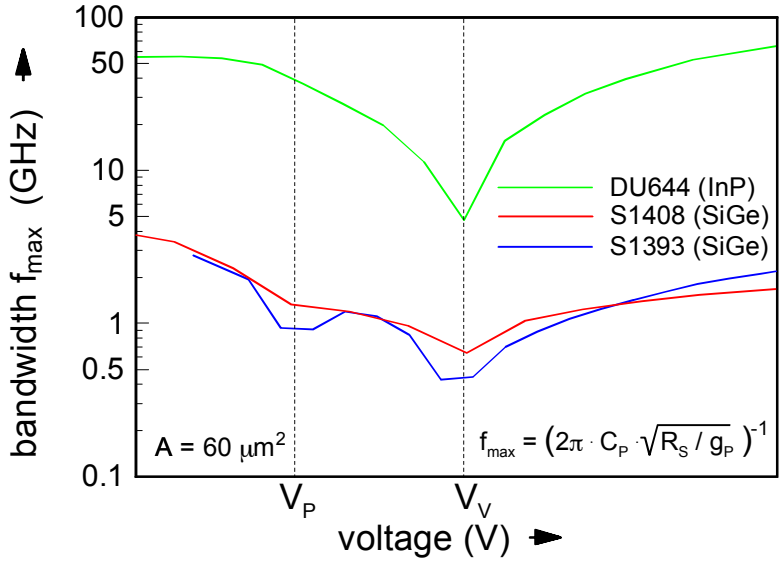


Fig. 5.5: Maximum oscillation frequency relatively to the peak- and valley-voltage of the SiGe-ITDs and of an InP-RTD based on the layer structure used in LOCOM.

WP 5.2: Exchange with Si-technology within MEL-ARI (SiQUIC)

The discussion of possible collaborations with the Si-industry (Daimler-Benz Research Center, Dr. Ulf König) and the Si-based quantum tunnelling project SiQUIC (Dr. D. Paul) took place at the beginning of the project. However, Daimler-Benz was restricted to analog applications and the SiQUIC project was not able to provide samples at this time. Therefore, LOCOM has started its own experimental work on Si tunnelling diodes as described in WP 5.1.

WP 6: Project management

Task 6.1 Project coordination

Each partner will be represented in the project committee by the project leader who has the main responsibility for his workpackage (cf. Form 5.3 of Technical Annex). To support the data exchange between the groups the coordinator will distribute the important data (circuit designs, measurement and simulation results, extracted SPICE parameters etc.) in electronic form. An annual technical meeting with external attendees will be organised by the coordinator who also prepares the status reports. The coordinator will be support by a research assistant (Wiss. Hilfskraft, 9h/Week) throughout the project.

Task 6.2 Coordinative Meetings

A LOCOM project committee will be set-up under the guidance of the coordinator and will meet at least every six months. Additional technical meetings will be organised by the involved partners.

Task 6.3 Web page

A web page will be generated by the UNIDO group.

Task 6.4 Status Reports

Every 12 month a status report will be organised by the coordinator. Each participant will provide the report on the workpackage which is under his responsibility(cf. Form 5.3 of Technical Annex).

Task 6.5 Final Report

The final report will be organised by the coordinator. Each participant will provide the report on the workpackage which is under his responsibility (cf. Form 5.3 of Technical Annex).

WP 6.1 -6.5

The exchange of data and information within LOCOM worked excellent. Subject of exchange were experimental device data, device models for circuit simulation, and physical I-V simulation results. Their frequent interdependence is obvious in any workpackage.

A list of meetings is given in the annex of this report.

The LOCOM web page "http://luzi.e-technik.uni-dortmund.de/~pacha/locom/locom1.html" was constructed in the beginning of the project and is currently updated.

A status report was provided in June 1999 and June 2000.

WP 7: Take-up of Results

The LOCOM proposal aims at a position in the pre-active scheme of the Nano-Scale integrated Circuit cluster of the MEL-ARI Initiative. The results have therefore to be implemented in the current and future activities (roadmap) of this Initiative. In general this will be provided by the development of novel circuits architectures allowing a reduced complexity i.e. wiring density. This is a pre-requisite of a future successful implementation of nano-scale devices in ultra-high density circuits. Most probably is this take-up for the future use of the Si-RTD exhibiting NDR which is the basic feature of the considered higher functionality devices.

Task 7.1 Knowledge Exchange: Technology

In order to keep the LOCOM consortium aligned with the international state-of-the-art especially in the USA and Japan existing personal contacts to leading groups i.e. Dr. A. Seabaugh (Raytheon Texas Instruments Systems) and Dr. M. Yamamoto (NTT) will be strengthen due to invitations to seminars and visits.

Task 7.2 Si-Industry and Si-Research

The Si-transfer will be supported due to intense contacts with the European Si-industry in order to assure the implementation of a technology which is most probable for transfer to Silicon. The agreement with Daimler-Benz (layer sequences for ESAKI-diodes) is of pronounced importance. The present status of possible Si-devices exhibiting NDR will be organised by intense contacts with the SiQUIC consortium of MEL ARI. This includes data- and knowledge exchange but also the assistance with state-of-the-art Si-technology for quantum electronics.

Task 7.3 Transfer to system level and knowledge dissemination within MEL ARI

For the transfer to system level the relation to the MEL-ARI proposal „ANSWERS“ will be important. LOCOM will provide a realistic technological data base for the work of this consortium. The co-operation with the complementary ANSWERS project is assured due to the work of the UNIDO group in both consortia. In addition, a special MEL-ARI session about these projects is planned within the application orientated Workshop “Innovative Circuits and Systems for Nanoelectronics“ which has been initiated by UNIDO.

WP 7.1 Knowledge Exchange: Technology

The hook-up of the LOCOM project to the state-of-the-art was done in 1998/1999. The labs of leading scientists in USA (Raytheon Texas Instruments, University of Michigan, Sandia Labs, Hughes Research Labs, CA), and Japan (NTT) were visited by LOCOM members (C. Pacha, W. Prost, and F.-J. Tegude). Finally, Dr. Klimeck, one of the inventors of the NEMO simulation software for quantum devices, gave seminar in Duisburg. Moreover, LOCOM member published numerous papers and discussed their work on leading international conferences (cf. section LOCOM references).

WP 7.2 Si-Industry and Si-Research

There was a lack of Si-based quantum electronic devices available at the beginning of the LOCOM project which inhibit a direct collaboration with partners in Si-based research and industry. As a consequence LOCOM has produced its own Si-based quantum device and has discussed a possible take-up of results in terms of high-speed digital filtering and hearing aid-manufacture.

Suggested that the final LOCOM demonstrator "Full Adder" is available with the following features:

- speed > 1 GBit/s,
- supply voltage < 0.7 V,

the following possible applications were explored within the last year:

- high speed numeric applications
- hearing-aid manufacture

The Full Adder is the basic computing element for any numeric operation and may replace together with simple shift operations nearly all mathematical functions. Prof. Goetze from the University of Dortmund, Institute of Informatics, is working on this subject and presented a seminar to the LOCOM partners discussing this aspect. We agreed to further explore the possible application of the Full Adder after availability for this purpose.

However, this aspect is more a "Take-up of Results", than a direct path to manufacture. This path has been explored in a visit at Siemens, Hearing-Aid Production, in Erlangen, in December 1999. Dr. Holube (Siemens) and Dr. Prost discussed the possible application of LOCOM circuits with following results:

The low supply voltage is clearly below the lowest available CMOS technology (> 1 V at reduced speed data, standard > 1.3 V). The provided high speed is of interest for improved digital signal processing. However, the available VLSI CMOS technology allows a massive parallel processing of data at reduced speed and with overall lower power consumption.

A further severe arguments against the use of any alternative technology is the availability of a set of numerous circuits (e.g. memory, A/D- D/A converters, power amplifier...). In addition, in order to reduce development costs there are in existing fabrication lines no developments teams available taking up novel technologies at a somewhat basic status.

In conclusion, in order to transfer LOCOM circuits to production further development steps are necessary and the aspect of high speed numeric operations for digital signal processing is assumed to be very promising for the next future.

WP 7.3 Transfer to system level and knowledge dissemination within MEL ARI

The excellent exchange with the ANSWERS project was the basis of the success of LOCOM and vice versa because LOCOM was the only source for experimental data for nanoelectronic circuit design within the ANSWERS project.

LOCOM has organised the July 1999 MEL-ARI/NID workshop in Duisburg, the “Innovative Circuits and Systems for Nanoelectronics“ in Dortmund, and has substantially contributed (C. Pacha, W. Prost) to the 1999 and the 2000 edition of the NID roadmap.

References

References WP1- WP5

Billen K, Wilkinson VA, Kelly MJ; Semicond. Sci. Technol., 12, pp. 894ff (1997).

Broekaert TPE, Lee W, Fonstad C G; *Pseudomorphic $In_{0.53}Ga_{0.47}As/AlAs/InAs$ resonant tunnelling diodes with peak-to-valley current ratios of 30 at room temperature*, Applied Physics Letters, vol.53, no.16, pp.1545-1547, 1988.

Brugger H, Meiners U, Wölk C, Deufel R, Schroth J, Förster A, Lüth H; *High Quality GaAs-Based Resonant Tunnelling Diodes for High Frequency Device Applications,* Proceedings of the 13th IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Cornell University, 5.-7, pp. 39–48, 1991.

Chen K, Meazawa K, Yamamoto M; *InP Based High Performance Monostable-Bistable Transition Logic Elements (MOBILE's) Using Integrated Multiple-Input Resonant-Tunnelling Devices*, IEEE Electron Device Lett., vol. 17, no. 3, pp. 127-129, 1996.

Chen CL, Mathews RH, Mahoney LJ, Maki PA, Molvar KM, Sage JP, Fitch GL, Sollner TCLG; *New Self-Aligned Planar Resonant-Tunnelling Diodes for Monolithic Circuits*, IEEE Electron Device Lett., vol. 18, no. 10, pp. 489-491, 1997.

Chuang SL; *Physics of optoelectronic devices*, John Wiley & Sons, Inc., 1995.

Duschl R, Schmidt OG, Eberl K; *Epitaxially grown Si/SiGe interband tunnelling diodes with high room-temperature peak-to-valley ratio*, Applied Physics Letters, vol. 76(7), pp. 879-881 (2000).

Fjeldly TA, Ytterdal T, Shur MS; *Introduction to Device Modeling and Circuit Simulation*, John Wiley & Sons, New York, 1998.

Förster A, Lange J, Gerthsen D, Dieker C, Lüth H; *Effect of interface roughness and scattering on the performance of AlAs/InGaAs resonant tunnelling diodes*, J. Vac. Sci. Technol. B11(4), p.1743 (1993).

Förster A, Lange J, Gerthsen D, Dieker C, Lüth H; *The effect of growth temperature on AlAs/GaAs resonant tunnelling diodes*, J. Phys. D: Appl. Phys. 27, pp. 175–178 (1994).

Förster A, Griebel M, Indlekofer M, Lüth H; *Transport through a buried double barrier single electron transistor at low temperatures*, Physica E, 2 (1-4), p.502 (1998).

Förster A; *Resonant Tunnelling Diodes Operating as Modern Quantum Transport Devices*, Proceedings of the Tenth International Workshop on the Physics of Semiconductor Devices, Delhi, p. 966, Allied Publisher LTD., New Delhi, ISBN 81-7023-997-4, 2000.

Goldberg DE; *Genetic algorithm in search, optimiszation, and machine learning*, Addison-Wesley Publishing Company, Reading, Mass (1989).

Griebel M, Indlekofer KM, Förster A, Lüth H; *Transport properties of gated resonant tunnelling diodes in the single electron regime*, Journal of Applied Physics 84 (12) 6718 (1998).

Griebel M, Indlekofer KM, Förster A, Lüth H*; Single Electron Transport in Resonant Tunnelling Diodes Laterally Confined by Ion Implantation*, J. Phys. D: Appl. Phys. 32 1729 (1999).

Haase M, Prost W, Velling P, Liu Q, Tegude FJ*; HR XRD for the analysis of ultrathin centrosymmetric strained DB-RTD heterostructures,* Thin Solid Films 319 pp. 25-28, 1998.

Hayden RK, Kelly MJ; *Tunnelling statistics and the manufacturability of semiconductor tunnel devices*, accept. Proc. 3rd Internat. Conf. on Materials for Microelectronics, Dublin October 2000.

Hayden RK, Missous M, Kelly MJ, *Epitaxial growth method for precision fabrication of heterostructure devices*, submitted to Electronics Letters.

Hendriks AMPJ, Magnus W, van de Roer TG; *Accurate Modelling of the Accumulation Region of Double Barrier Resonant Tunnelling Diode*, Solid-State Electronics, vol.39, no.5, pp.703-712, 1996.

Ismail K, Meyerson BS, Wang PJ; *Electron resonant tunnelling in Si/SiGe double barrier diodes*, Applied Physics Letters, vol. 59(8), pp. 973-975 (1991).

Kane EO; *Band structure of indium antimonide*, J.Phys.Chem.Solids, vol.1, pp.249-261, 1957.

Kane EO; *Theory of Tunnelling*, J. Appl. Phys., vol.32, no.1, p.83 ff., 1961.

Kelly MJ; *New statistical analysis of tunnel diode barriers*, Semicond. Sci. Technology 15 79-83 (2000).

Köpf C, Kosina H, Selberherr S; *Physical Models for Strained and Relaxed GaInAs Alloys: Band Structure and Low-Field Transport*, Solid-State Electronics, vol.41, no.8, pp.1139-1152, 1997.

Maezawa K, Mizutani T; *A New Resonant Tunnelling Logic Gate Employing Monostable-Bistable Transition*, Jpn. J. Appl. Phys., vol. 32, part 2, No. 1A/B, pp. L42 - L44, January 1993.

Matthews JW, Blakeslee AE; J. Crystal Growth 27, 118 (1974).

Mars DE, Yang L, Tan MRT, Rosser SJ; *Reproducible growth and applications of AlAs/GaAs double barrier resonant tunnelling diodes*, J. Vacuum Science and Technology, B 11 965-8 (1993).

Ohler C, Daniels C, Förster A, Lüth H; *Heterojunction band offsets and Schottky-barrier heights: Tersoff's theory in the presence of strain*, Physical Rev. B, vol.58, no.12, pp.7864-7871, 1998.

Pacha C, Auer U, Burwick C, Glösekötter P, Brennemann A, Prost W, Tegude FJ, Goser K; *Threshold Logic Circuit Design of Parallel Adders Using Resonant Tunnelling Devices*, accepted for publication, Sept. 1999, IEEE Transactions on Very Large Scale Integration Systems, vol. 8, no. 5, pp. 558-572, 2000.

Palankovski V, Kaiblinger-Grujin G, Selberherr S; *Study of dopant-dependent band gap narrowing in compound semiconductor devices*, Material Science and Engineering, B66, pp.46-49, 1999.

Pollak FH; *Effects of Homogeneous Strain on the Electronic and Vibrational Levels in Semiconductors*, in T.P.Pearsall, editor, Strained-Layer Superlattices: Physics, vol.32 of Semiconductors and Semimetals, chap.2, pp.17-53, Academic Press, 1990.

Prost W, Auer U, Tegude FJ, Janßen G, van der Roer T, Pacha C, Goser K; *Manufacturability and Robust Design of Nanoelectronic Logic Circuits based on Resonant Tunnelling Diodes*, Int. J. Circ. Theor. Appl, Special Issue on Nanoelectronic Circuits, vol. 28, pp. 537-552, 2000.

Shiraishi Y et al., J. Appl. Phys. 76 (9), pp. 5099 ff (1994).

Souifi A, Brémond G, Benyattou T, Guillot G; *Band-gap narrowing determination by photoluminescence on strained B-doped $Si_{0.82}Ge_{0.18}$ layers grown on Si*, Appl. Phys. Lett., vol.62, no.7, p.2986, 1993.

Stock J, Indlekofer M, Malindretos J, Förster A, Lüth H; *A Vertical Resonant Tunnelling Transistor for Application in Digital Logic Circuits*, accepted IEEE Trans. Electron Devices (2001).

Syme RT; *Microwave detection using GaAs/AlAs tunnel structures*, GEC J Research, 11 12-23 (1993).

Tsao JY, Dodson BW; Appl. Phys. Lett. 53(10), 848 (1988).

Wilkinson VA, Kelly MJ, Carr M; *Tunnel devices are not yet manufacturable*, Semiconductor Science and Technology 12 91-99 and references therein (1997).

Ziegler J F; http://www.research.ibm.com/ionbeams, Yorktown, NY, 10598, USA.

LOCOM Publications

Key Papers

WP1: Pacha C, Auer U, Burwick C, Glösekötter P, Goser K, Prost W, Brennemann A, Tegude FJ; *Threshold Logic Circuit Design of Parallel Adders Using Resonant Tunnelling Devices*, IEEE Transactions on Very Large Scale Integration Systems, Special Issue on Ultra-Scale Computing, vol.8, no.5, pp558-572, October 2000.

WP2: Prost W, Auer U, Tegude FJ, Pacha C, Goser K, Duschl R, Eberl K, Schmidt OG; *Tunnelling Diode Technology*, International Symposium on Multiple-Valued Logic, ISMVL 2001, Warshaw, May 2001, acc. for publ. IEEE Computer Society.

WP3: Prost W, Auer U, Tegude FJ, Pacha C, Goser K, Janßen G, van der Roer T; *Manufacturability and Robust Design of Nanoelectronic Logic Circuits based on Resonant Tunnelling Diodes*, Int. J. Circ. Theor. Appl, Special Issue on Nanoelectronic Circuits, vol. 28, pp. 537-552, 2000.

WP4: Stock J, Indlekofer M, Malindretos J, Förster A, Lüth H; *A Vertical Resonant Tunnelling Transistor for Application in Digital Logic Circuits*, accepted for publication in IEEE Trans. Electron Devices (2001).

WP5: Auer U, Prost W, Tegude FJ, Duschl R, Eberl K; *Low-voltage MOBILE logic module based on Si/SiGe Interband Tunnelling Diodes*, submitted to Electron Device Letters.

Publications on RTD Devices and Material Evaluation

Auer U, Prost W, Tegude FJ, Duschl R, Eberl K; *Low-voltage MOBILE logic module based on Si/SiGe Interband Tunnelling Diodes*, submitted to Electron Device Letters.

Förster A; *Resonant Tunnelling Diodes Operating as Modern Quantum Transport Devices*, Proceedings of the Tenth International Workshop on the Physics of Semiconductor Devices, Delhi, p. 966, Allied Publisher LTD., New Delhi, ISBN 81-7023-997-4, 2000.

Förster A, Griebel M, Indlekofer M, Lüth H; *Transport through a buried double barrier single electron transistor at low temperatures*, Physica E, 2 (1-4), 502 (1998).

Förster A, Lüth H, Schäpers T; *Quantenelektronik: Die neue Welt*, Spektum der Wissenschaft, pp. 90-93, Juni 1999.

Janßen G, Velling P, Auer U, Prost W, Tegude FJ; *Circuit Simulation of bias dependent NAND/NOR operation realised by a single Resonant Tunnelling Transistor*, submitted to IEEE J. Solid-State Circuits, 2001.

Griebel M, Indlekofer KM, Förster A, Lüth H; *Single Electron Transport in Resonant Tunnelling Diodes Laterally Confined by Ion Implantation,* Journal of Physics D: Appl. Phys. 32 1729 (1999).

Griebel M, Indlekofer KM, Förster A, Lüth H; *Transport properties of gated resonant tunnelling diodes in the single electron regime*, Journal of Applied Physics 84(12) 6718 (1998).

Haase M, Prost W, Velling P, Liu Q, Tegude FJ; *HR XRD for the analysis of ultrathin centrosymmetric strained DB-RTD heterostructures,* Thin Solid Films 319 pp. 25-28, 1998.

Hayden RK, Kelly MJ, Tunnelling statistics and the manufacturability of s emiconductor tunnel devices, to appear in the proceedings of the 3rd International Conference on Materials for Microelectronics, Dublin October 2000.

Hayden RK, Missous M, Kelly MJ; *Epitaxial growth method for precision fabrication of heterostructure devices*, submitted to Electronics letters.

Kelly MJ; *New statistical analysis of tunnel diode barriers*, Semicond. Sci. Technology 15 79-83 (2000).

Prost W, Auer U, Tegude FJ, Pacha C, Goser K, Janßen G, van der Roer T; *Manufacturability and Robust Design of Nanoelectronic Logic Circuits based on Resonant Tunnelling Diodes*, Int. J. Circ. Theor. Appl, Special Issue on Nanoelectronic Circuits, vol. 28, pp. 537-552, 2000.

Prost W, Tegude FJ; *Tunnelstrukturen - Grundlagen und Baulemente* -, in "Nanostrukturen in

Halbleitern“ des Graduiertenkolleges “Metrologie in Physik und Technik“, Herausgeber Schlachetzki A, Kunzmann H, PTB-F-31, ISBN 3-89701-115-8, Braunschweig, 1998.

Stock J, Indlekofer M, Malindretos J, Förster A, Lüth H; *A Vertical Resonant Tunnelling Transistor for Application in Digital Logic Circuits*, accepted for publication in IEEE Trans. Electron Devices (2001).

Vitusevich SA, Förster A, Belyaev AE, *Glavin BA, Indlekofer KM, Lüth H, *Konakova RV; *Optically controlled 2D tunnelling in GaAs delta-doped p-n junction, Semiconductor physics*, Quantum electronics & Optoelectronics, 2 (1) 7 (1999). *) National Academy of Science of Ukraine.

Vitusevich SA, Förster A, *Belyaev AE, Indlekofer KM, Lüth H, *Konakova RV; *Intrinsic Bistability Effect in Delta Doped Tunnelling Diodes*, Proceedings of the 28th International school on Physics of Semiconducting compounds Jaszowiec, Poland 171 (1999). *) National Academy of Science of Ukraine.

Vitusevich SA, Förster A, Belyaev AE, Indlekofer KM, Lüth H, Konakova RV; *Resonant tunnelling effect in delta p-n GaAs junction*, Microelectronic Engineering *46*(1-4) 169 (1999).

Vitusevich SA, Förster A, Indlekofer KM, Lüth H, Belyaev AE, Glavin BA, Konakova RV; *Tunnelling Through X-Valley-Related Impurity States in GaAs/AlAs Resonant-Tunnelling Diodes*, Phys. Rev. B *61*(16) 10898 (2000).

Vitusevich SA, Förster A, Reetz W, Lüth H, Belyaev AE, Danylyuk SV; *Spectral Responsivity of single-quantum-well photodetectors*, Applied Physics Letter *77*(1) 16 (2000).

Publication on RTD-HFET circuits

Auer U, Prost W, Pacha C, Brennemann A, Goser K, Tegude FJ; *Novel MOBILE Logic Gates,* Microelectronics Advanced Research Initiative/Nanoscale Information Devices, 4th Annual Workshop, Gerhard-Mercator-Universität Duisburg, 7.-9. July 1999.

Glösekötter P, Pacha C, Goser K; *Associative Matrix for Nanoscale Integrated Circuits*, Proceedings of the 7th International Conference on Microelectronics for Neural, Fuzzy and Bio-Inspired Systems (MircoNeuro), Granada, Spain, March 1999, IEEE Computer Society Press, Los Alamitos, CA, pp. 352-358.

Goser K, Pacha C; *System and Circuit Aspects of Nanoelectronics* (invited paper), ESSCIRC'98 - Pacha C, Goser K; *Adiabatic Switching of Resonant Tunnelling Devices,* Proceedings of the 3rd Workshop on Innovative Circuits and Systems for Nanoelectronics, TU München, 5.-6. October 1998.

Janßen G, van de Roer TG, Prost W, Auer U, Tegude FJ, Pacha C, Glösekötter P, Goser K, Förster A, Malindretos J, Kelly MJ; *Calculation of the well charge in resonant tunnelling diodes and the impact of the well charge on the device capacitance*, 12th III-V Semiconductor Device Simulation Workshop, Oct. 10-11, Duisburg, Germany, 2000.

Pacha C, Auer U, Burwick C, Glösekötter P, Goser K, Prost W, Brennemann A, Tegude FJ; *Threshold Logic Circuit Design of Parallel Adders Using Resonant Tunnelling Devices,* IEEE Transactions on Very Large Scale Integration Systems, Special Issue on Ultra-Scale Computing, vol. 8, no. 5, pp. 558-572, October 2000.

Pacha C, Kessler O, Goser K, Prost W, Brennemann A, Auer U, Tegude FJ; *Parallel Adder Design with Reduced Circuit Complexity Using Resonant Tunnelling Devices and Threshold Logic,* Kluver Academic Publishers**,** Analog Integrated Circuits and Signal Processing, 24, pp. 7-25, 2000.

Pacha C, Goser K; *Technology Roadmap for Nanoelectronics, Chapter 4: Circuits and Systems,* European Commission, IST Program, Microelectronics Advanced Research Initiative, Editors: R. Compano, L. Molenkamp and D-J. Paul, April 1999.

Pacha C, Glösekötter P, Goser K, Prost W, Auer U, Tegude FJ; *Resonant Tunnelling Transistors for Threshold Logic Circuit Applications,* Proceeding of the 9th Great Lakes Symposium on VLSI, Ann Arbor, MI, IEEE Computer Society Press, Los Alamitos, CA, pp. 344-345, 1999.

Pacha C, Goser K, Brennemann A, Prost W; *A Threshold Logic Full Adder Based on Resonant Tunnelling Transistors,* Procceedings of ESSCIRC'98 - European Solid-State Circuits

Conference, The Hague, September 1998, Edition Frontieres, pp. 428-431, 1998.

Pacha C, Glösekötter P, Goser K; *Adiabatic Switching and Power Dissipation of Dynamic Resonant Tunnelling Device Logic Circuits*, 3rd Workshop on Innovative Circuits and Systems for Nanoelectronics, Munich, 1998.

Prost W, Velling P, Janßen G, Auer U, Brennemann A, Glösekötter P, Goser K, Tegude FJ; *Resonant-Tunnelling 3-Terminal Devices for High-Speed Logic Application*, 24th WOCSDICE, Aegean Sea, Greece, May 29 - June 2, 2000.

Prost W, Auer U, Pacha C, Brennemann A, Goser K, Tegude FJ; *Novel MOBILE Gates with Low-Power, Relaxed Parameter Sensitivity, and Increased Driving Capability,* 11th Intern. Conf. on Indium Phosphide and Related Materials, Davos, pp. 415-418, 1999.

Prost W, Auer U, Pacha C, Janßen G, Bertenburg RM, Brockerhoff W, Goser K, Tegude FJ; *InP-based HFET's and RTDs for High Speed Digital Circuitry,* International Symposium on Signals, Systems and Electronics, Pisa, IEEE Catalog No 98EX167, pp. 45-49, 1998.

Prost W, Velling P, Auer U, Brennemann A, Pacha C, Goser K, Tegude FJ; *Assessment and the Impact of Structural Paramters and Device Technology on Resonant Tunnelling Diode Characteristics,* 4th International Workshop on Expert Evaluation and Control of Compound Semiconductor Materials and Technologies (EXMATEC), Cardiff, UK, June 1998.

Prost W, Pacha C, Brennemann A, Goser K, Tegude FJ; *Manufacturability and Prospects of RTD/HFETs for Digital Circuitry of Reduced Complexity on InP,* 22nd Workshop on Compound Semiconductor Devices and Integrated Circuits (WOSDICE), Zeuthen, pp. 130, 1998.

Thomas M., Pacha C, Goser K; *Parameter Determination for Nano-Scale Modelling*, Proceedings of the European Solid-State Circuits Conference, The Hague, NL, pp. 18-29, September 1998.

Invited papers and presentations

Goser K, Pacha C; *System and Circuit Aspects of Nanoelectronics,* Procceedings of ESSCIRC'98 - European Solid-State Circuits Conference, The Hague, Edition Frontieres, pp. 18-29, September 1998.

Janßen G, Prost W, Auer U, Tegude FJ, Pacha C, Gloesekoetter P, Goser K, van de Roer T, Foerster A, Malindretos J, Kelly MJ; *Logic Circuits with Reduced Complexity based on Devices with Higher Functionality*, SAFE (Semiconductor Advances for Future Electronics) Mierlo, Nov. 24-25, NL, 1999.

Prost W, Auer U, Tegude FJ, Janßen G, van der Roer T, Pacha C, Goser K; *Manufacturability and Robust Design of Nanoelectronic Logic Circuits based on Resonant Tunnelling Diodes*, Int. J. Circ. Theor. Appl, Special Issue on Nanoelectronic Circuits, vol. 28, pp. 537-552, 2000.

Prost W, Auer U, Pacha C, Janßen G, Bertenburg RM, Brockerhoff W, Goser K, Tegude FJ; *InP-based HFET's and RTDs for High Speed Digital Circuitry*, International Symposium on Signals, Systems, and Electronics, Pisa, Italy, September, 1998.

Prost W; *Resonanztunneldioden: Monolagen-Bauelemente für Schaltungen*, 15. DGKK-Workshop Epitaxie von III/V-Halbleitern, Bad Dürkheim, 11. Dezember 2000.

Prost W, Pacha C, Goser K, Tegude FJ; *Tunnelling Diode Technology*, International Symposium on Multiple-Valued Logic, ISMVL 2001, Warshaw, May 2001.

Invited Seminars

Brennemann A; *III/V-based Digital Circuits*, University of Notre Dame, USA, May 15th, 2000.

Förster A; *Resonante Tunneldioden in Anwendungen als moderne Quantenbauelemente*, Institut für Halbleitertechnik, TU Braunschweig (D), 18.1.2000.

Förster A; *Logic Units based on Resonant Tunnelling Devices*, Seminar of the Institute of Semiconductor Physics, NAUKI, Kiev (UK), 30.3.2000.

Pacha C, Goser K; *Resonant Tunnelling Device Logic Gates for Bit-Level Pipelined Arithmetic Circuits*, a) Raytheon Texas Instruments Systems, Corporate Research and Development, Dallas, TX,

March 8, 1999, b) Sandia National Laboratory, Nanoelectronics Group, Albuquerque, NM, March 10, 1999.

Pacha C; *Logic Circuit Design Using Nanoelectronic Devices*, Infineon Technologies AG, Corporate Research, March 4, 2000, Munich.

Prost W; *A novel MOBILE based logic element with low-power, relaxed parameter sensitivity, and increased driving capability*,
a) Jet Propulsion Laboratory, California Institute of Technology, High Performance Computer Systems and Applications Group, Pasadena, CA, June 1999; b) Hughes Research Laboratories, Malibu, CA, June 1999.

Prost W; *Zum Einsatz von Resonanztunneldioden in Digitalschaltungen*, Max-Planck-Insitut für Festkörperforschung, Stuttgart, 02.11.1999.

Prost W; *Circuit Applications of Resonant Tunnelling Diodes*, Université de Provences, Institut Charles Fabry, Marseille, 14.01.2000.

Prost W; *Circuit Applications of Resonant Tunnelling Diodes*, Seminar at Universita' di Parma, Febr. 21, 2000.

Prost W; *A novel MOBILE based logic element with low-power, relaxed parameter sensitivity and increased driving capability*, a) Seminarvortrag HRL Laboratories, Malibu, CA, 24. Juni 1999. b) Seminar Jet Propulsion Lab, California Institute of Technology, Pasadena, CA, 25. Juni 1999.

Prost W; *III/V-Halbleiterheteroepitaxie und Entwicklung schaltungsrelevanter Resonanztunneldioden,* RWTH Aachen, Kolloquium der Fakultät für Elektrotechnik und Informationstechnik, Aachen, June 6, 2000.

Guest Seminars on LOCOM Meetings

Klimeck G, Bowen C, Boykin[1] T, Oyafuso[2] F, Carlos H, Salazar-Lazaro, Stoica A, Cwik T; Jet Propulsion Laboratory/California, Institute of Technology, 1)University of Alabama in Huntsville, 2)University of Illinois, *The Nanoelectronic Modeling Tool (NEMO) and its Expansion to High Performance Computing*, Gerhard-Mercator-Universität Duisburg, 25.11.1998.

Prof. Goetze; *Digital signal processing with shift & add*, Universität Dortmund; Institute of Informatics, Gerhard-Mercator-Universität, Prof. Götze gives an overview of digital signal processing with shift & add. He refers to transformations, CORDIC, approximations and scaling factor compensation. He shows simulation results of a quadrature mirror filter and a lattice filter. At the end he suggests an approximate implementation, Feb., 16th, 2000.

Keiper D; *MOVPE at KTH (Stockholm) for InP- and GaAs-based devices for fiber communication*, Gerhard-Mercator-University Duisburg, Royal Institute of Technology, Department of Electronics, Electrum 229, S-164 40 Kista-Sweden, Jan. 6th, 2000.
Abstract: After a short presentation of the Institute different MOVPE processes for InP- and GaAs-based devices are reviewed, focusing on the device-specific difficulties for the MOVPE growth. Furthermore, a new MOVPE process is presented using TBA and TBP in N_2 ambient instead of the toxic and gaseous AsH_3 and PH_3 in H_2 ambient and the advantageous and disadvantageous will be discussed.

Further publications of LOCOM members

Nano-scale circuit design and modelling

Förster A, Lüth H, Schäpers T; *Quantenelektronik: Die neue Welt*, Spektum der Wissenschaft, 90-93, Ausgabe Juni 1999.

Glösekötter P, Pacha C, Goser K; *Associative Matrix for Nano-scale Integrated Circuits*, Proceedings of the 7th International Conference on Microelectronics for Neural, Fuzzy and Bio-Inspired Systems (MircoNeuro), Granada, Spain, IEEE Computer Society Press, Los Alamitos, CA, pp. 352-358, March 1999.

Glösekötter P, Pacha C, Goser K; *Design of Arithmetic Circuits Using the RTBT*, ITG-Fachbericht 162, Mikroelektronik für die Informationstechnik , ISBN 3-8007-2586-X, pp. 147 – 150, Nov. 20 - 21, 2000.

Glösekötter P, Pacha C, Goser K; *Threshold Logic Circuit Design using the RTBT*, Kleinheubacher Berichte, Sep. 25 - 29, 2000.

Glösekötter P, Pacha C, Goser K, Wirth G, Prost W, Auer U, Agethen M, Velling P, Tegude FJ; *Digital Circuit Design Based on the Resonant-Tunnelling-Hetero-Junction-Bipolar-Transistor*, SBCCI, Sep. 1. - 24, 2000, Manaus, Brasil.

Indlekofer KM, Lüth H; *Many-particle density-matrix approach to a quantum dot system for the strong electron accumulation case*, Phys. Rev. B 62(19) 13016 (2000).

Prost W, Kruis FE, Otten F, Nielsch K, Rellinghaus B, Auer U, Peled A, Wassermann EF, Fissan H, Tegude FJ; *Monodisperse Aerosol Particle Deposition: Prospects for Nanoelectronics,* J Microelectr. Eng., 41/42 535-538 (1998).

Stock J, Malindretos J, Indlekofer M, Pöttgens M, Griebel* M, Förster A, Lüth H; *Ein vertikaler resonanter Tunneltransistor im System GaAs/AlAs für den Einsatz in digitalen Logikschaltkreisen*, DPG Frühjahrstagung, Regensburg (D), 27.03.2000 – 31.03.2000. *) Max-Planck-Institut für Festkörperforschung, Stuttgart .

Thomas M, Pacha C, Goser K; *Parameter Determination for Nano-Scale Modelling*, Proceedings of the International Conference on Evolutionary Computation, Dortmund, Germany, May 1999.

Velling P, Janßen G, Auer U, Prost W, Tegude FJ; *Logic NAND/NOR circuit using single InP-based RTBT*, Electron. Lett., 34(25), pp.2390-2392 (1998).