



FT-EA

IST-2001-38930

Using Fault-Tolerance techniques to combat Electrical Aspects in deep sub micron IC Technology

Final Report

Covering period 01-01-2003 - 30-06-2004

Report Version: Final (update)

Report Preparation Date: 14-2-2005

Classification: Public

Contract Start Date: 01-01-2003

Duration: 18 Months

Project Co-ordinator: André Nieuwland

Partners: Philips Research Laboratories Eindhoven

IROC Technologies

University of Bologna



Project funded by the European Community under the "Information Society Technologies" Programme (1998-2002)

Table of Content

1. Manpower overview	3
2. Project overview	4
3. Summary of project results and achievements	8
4. Dissemination and exploitation.....	10
4.1 Dissemination activities.....	10
4.2 Exploitation activities.....	10
5. Project deliverables	11
6. Conclusions.....	12
7. Appendix: Published Papers	13
7.1 Conference Papers originating from FT-EA project	13
7.2 Journal papers originating from FT-EA project	13
7.3 Patent applications originating from FT-EA project.....	13

1. Manpower overview

MANPOWER SPENT: (Jan/Jun 2004)

Actually Spent Human Resource Allocation

Partner	WP1	WP2	WP3	WP4	Total
Philips NL	0	0	1	4	5
University of Bologna	0	0	5	6	11
IROC Technologies	0	0	5	2	7
Total	0	0	11	12	23
<i>Planned</i>	<i>0</i>	<i>0</i>	<i>10</i>	<i>11</i>	<i>21</i>

(actual manmonths are rounded best estimates; final accurate manpower are given in the cost claims)

MANPOWER SPENT: (Jan 2003/Jun 2004)

Actually Spent Human Resource Allocation

Partner	WP1	WP2	WP3	WP4	Total
Philips NL	5	5	5	4	19
University of Bologna	9	9	8	6	32
IROC Technologies	7	6	6	2	21
Total	21	20	19	12	72
<i>Planned</i>	<i>20</i>	<i>20</i>	<i>19</i>	<i>11</i>	<i>70</i>

(actual manmonths are rounded best estimates; final accurate manpower are given in the cost claims)

2. Project overview

In this project we studied the possible use of error correcting codes to also solve electrical problems such as cross-talk, power consumption and simultaneously switching noise. It was unknown that, although providing similar error protection, different error correcting codes have drastic effects on the electrical problems. Although the codes look similar at first hand, their effect on problems such as cross talk, power consumption, etc. is very different indeed! These findings are the result of an initial study where we needed fault tolerance. We discovered that in a novel way, the code can be chosen to combat the majority of the above mentioned electrical problems with no extra cost. This means that we can obtain large energy savings and avoid cross-talk, just by using the tools developed during the project to implement fault-tolerance in a different way! Though we were able to alleviate the problem of simultaneously switching outputs by combining fault tolerant coding with bus-invert coding, we found that this step had negative impact with respect to power consumption and cross-talk reduction.

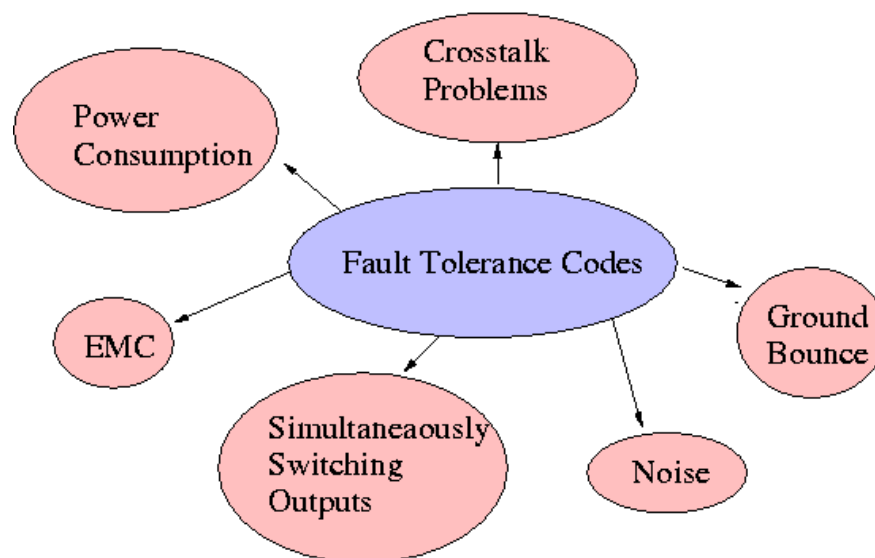


Figure 1: By choosing special codes for the mandatory Fault Tolerance on future ICs, a number of electrical aspects that will pose problems can be automatically covered

For instance, considering the combination of low power consumption (one of the major aspects of portable electronics) and fault-tolerant issues (which is mandatory for health care, automotive safety systems, etc., and which will become necessary also for next generation consumer electronics), an innovative approach was carried on, aimed at developing coding techniques which provide fault-tolerance and allow energy savings. They are based on the construction of error correcting codes whose code words are computed in such a way that the most power consuming transitions between two adjacent bit-lines never occur.

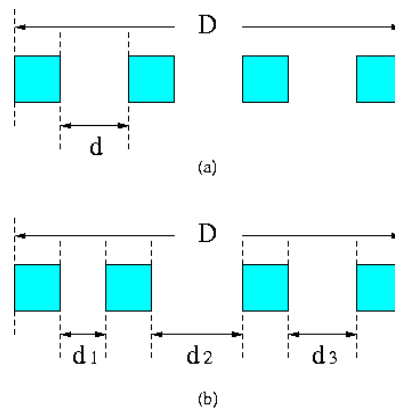


Figure 2: Different bus layout techniques: (a) conventional spacing; (b) intelligent spacing to reduce power consumption.

The outstanding advantages achieved using the proposed ECC were then further optimised through the application of intelligent inter-wire spacing. In particular, adjacent wires which carry highly correlated signals (i.e., signals likely to be equal to each other) can be kept at a lower distance than wires carrying uncorrelated (or opposite correlated) signals. In this way, the amount of *effective* inter-wire mutual capacitance to be charged during bus activity can be drastically reduced, as adjacent wires will most likely carry equal voltage levels. This combined approach is leading to impressive energy savings! Figure 2 illustrates intelligent spacing with a simple example of a 4 wire bus. Whereas the conventional design would have equal spacing (a), the intelligent spacing (b) has the highly identical-correlated signals on a minimum spacing (d_1), and the spacing between more opposite or uncorrelated signals on larger distances (d_2). The spacing towards lines with other correlation coefficients or shield-wires can yet be different as well (spacing d_3).

With the newly developed Modified Dual Rail (MDR) coding we exploited exactly this property. By having the check-bit of each data-bit chosen to be identical and placed on minimum spacing with respect to the corresponding data bit, and by having the final parity bit duplicated and placed as a separate pair, we optimised the bus with respect to the reduction of the *effective* mutual coupling. Comparing the results with a Hamming coded bus using the same area, it has been shown that we gain significantly in reduction of power, delay, and cross-talk. This was quite counter-intuitive, as the number of check-bits of the developed codes is higher than with standard Hamming codes, which have a minimum number of check bits with respect to the number of data bits and fault protection. This result is even more striking when we realise that the smaller number of bus-wires required for Hamming codes have the advantage of an increased area available for larger spacing between the wires (hence reduced mutual capacitance). Despite of the smaller spacing due to the larger number of wires on the same area, the newly developed codes outperform Hamming codes.

Very promising results have been achieved, and the resultant coding scheme has been patented. We have shown that by applying Dual-Rail (DR) coding, 14% can be saved on power with respect to a Hamming encoded bus using the same area, despite the larger number of wires for the DR bus! At the same time, we were able to reduce the cross-talk induced delay and cross-talk induced peak-voltage by almost 40% using the DR-technique and the co-developed layout technique. Further development resulted in modified dual rail (MDR) coding which has an additional parity wire compared to the DR method. Together with a matching layout technique, MDR resulted in even a 45% reduction in cross-talk induced delay, whereas the standard Hamming coding using the same optimal lay-out technique resulted only in a 10% improvement. The improvement of MDR over Hamming is clearly indicated in Figure 3, where the relative cross talk delay reduction is plotted as a function of the wire spacing, considering the same area for the bus. As the spacing is increasing beyond the minimum bus footprint, the layout optimisation starts to work and the performance of MDR increases. For very large spacing, the mutual coupling loses the negative influence, and the advantage of MDR coding lies completely in the pair-wise placement of the signal wire and corresponding check-bit on

minimum spacing. Due to the vicinity of the highly correlated wires, the ground and fringe capacitances are effectively reduced, resulting in a faster propagation speed of the signals for an MDR bus as compared to a Hamming bus, considering the same bus area (footprint).

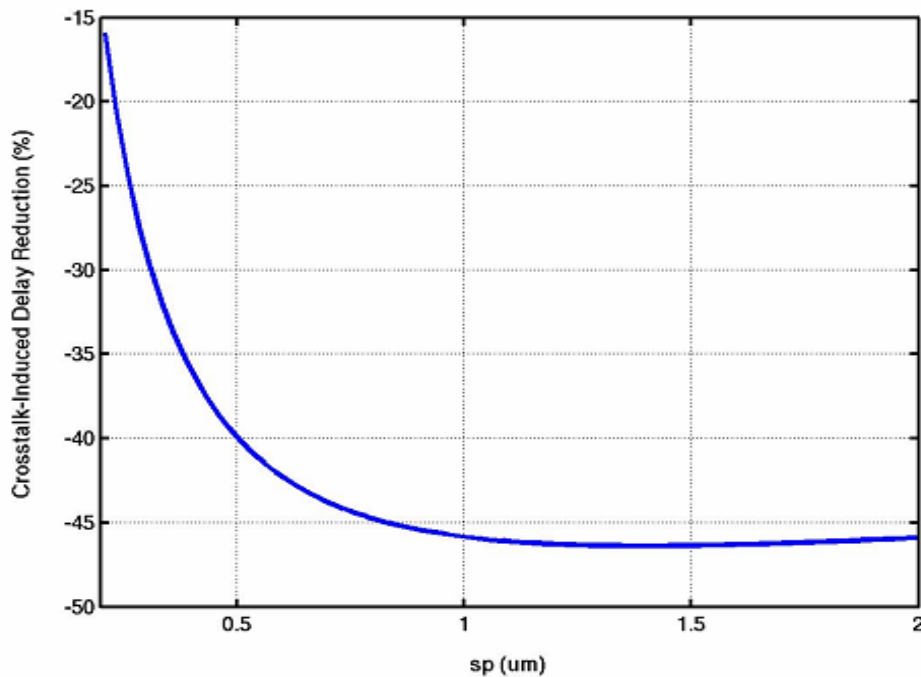


Figure 3: Relative improvement of MDR code with respect to Hamming code as function of wire spacing

The last part of the project aimed at developing a code which has inherently low simultaneously switching output (SSO) noise. SSO noise is induced by the switching outputs, because bus-drivers suddenly draw a large current from the power supply to charge the bus-wires. The result is that the on-chip supply voltage is suddenly lowered, resulting in less drive strength for the surrounding logic and bus-drivers (possibly causing signal dependent delay faults). Furthermore, due to the lower supply voltage, there is a reduced signal integrity as a consequence of the lower noise margin. This may cause bit errors in logic and memory elements and faulty behaviour of the system. Within the project we focussed on obtaining a deep insight in the causes and nature of the SSO noise (what are the dominant factors) and on the development of codes with low switching activity. After fully understanding the influence of the current loops and the role of parasitic capacitances, we were able to derive a model for SSO estimation which was implement-able in the design tool. We found that capacitance modelling is playing an important role, and that on-chip capacitances lead to different code sensitivity than off-chip capacitances. For on-chip busses, the capacitances have to be modelled as a split-load model towards power and ground, which had the effect that the direction of the switching (up or down) was only marginally important. For off-chip busses, where most of the capacitance will be towards ground, there is an asymmetry with respect to the impact of up- versus down-transitions (up is worse). In both cases, we found to our surprise that the transition activity between adjacent wires (mutual activity) does not play a role of importance as we expected before hand. We found that the dominant factor in the noise is the drive strength of the buffer in combination with the (parasitic) current loops. We have been investigating different codes for their SSO behaviour, but did not succeed within the time available within the project in finding or developing a code which solved the problem and was implement-able with limited complexity (to avoid excessive performance loss and increase in power consumption). Therefore, we resided to combining bus-invert coding (reducing SSO noise with about 50%) with fault tolerant encoding. An efficient implementation has been developed of integrated bus-invert Hamming coder, which is currently in the process of being patented.

The knowledge and fault tolerant codes developed within this project have been implemented in a fault tolerant bus design tool, called B-RoCKIT. The tool allows to quickly explore the power consumption and cross-talk behaviour of different fault tolerant codes and for different bus-footprints. Furthermore, it optimises the spacing between the bus-wires given the footprint, and when the designer is satisfied with the results, the tool generates the RTL hardware description of the encoder, decoder and bus structure, which can be fed into a synthesis tool for the final IC design. Additionally, the designer can have the tool evaluate the simultaneously switching output (SSO) noise of the corresponding codes. Based upon that outcome, the decision can be made whether to incorporate bus-invert coding into the fault tolerant bus en-/decoder or not. Based upon this decision, the tool will also generate the RTL description for that part of the fault tolerant encoder and decoder.

The unification of the research activities aimed on cross-talk, power consumption and SSO noise has found its destiny in the tool developed within the project. Whereas cross talk and power consumption reduction were obtained using the same coding technology, SSO noise requirements were such that the reduction in power consumption and cross-talk were compromised. By having the tool calculating and presenting the different options to the designer, the designer can easily make the trade off between the options. In this way, the optimal choice with respect to area, cross talk, power and SSO noise, depending on implicit or additional constraints and the view of the designer, is obtained. After the designer has made his choice, the tool will generate the required hardware description, ready for automated layout tools.

As the tool can be controlled by command line parameters and by script-files, the tool is easy to use in various environments, and can be easily incorporated in design flows and/or used for iterative design optimisation.

3. Summary of project results and achievements

1. Reduction of power consumption in busses
By the development and implementation of dual-rail coding together with an appropriate lay-out technique, more than 10% reduction in bus-power can be obtained with respect to a Hamming code with the same error correction ability using the same bus footprint. Moreover, a power estimation model has been developed for obtaining the bus power in a very fast way, without the need for SPICE-like simulations. This model, of which the accuracy has been verified to be within 5% with respect to SPICE, has been implemented in the design tool, B-RoCKIT. For large bus-footprints, and un-buffered busses, dual rail performs best. For wide buffered busses Hamming outperforms dual-rail encoding to the smaller number of repeaters required. When for speed reasons, the busses are split in sub-busses of 4 bits, 14% power consumption reduction can be obtained by using dual-rail encoding instead of Hamming coding. This figure includes the active elements such as drivers and encoding circuitry. The gains in power-delay product of the novel dual-rail encoding is substantially better: 37% less than Hamming, a clear benefit of this coding approach.
2. Reduction of cross-talk.
To reduce cross-talk effects, the dual-rail code has been modified into a *modified dual-rail code*, and an optimal layout technique has been invented resulting in a very high cross-talk reduction. The reduction in cross-talk peak-voltage and cross-talk induced delay is obtained by reducing the *effective* coupling capacitance. For the Modified Dual-Rail coding, all signals are laid-out in pairs with their corresponding check-bit on minimum spacing, as well as the parity signal with its corresponding check bit, whereas all pairs are laid-out with the maximum spacing available considering the bus footprint. The application of the developed optimal lay-out technique for Hamming coding only results in 10% reduction of cross-talk induced delay, whereas the same technique brought 34% reduction in cross-talk induced delay for the dual-rail code. The newly developed modified dual-rail (MDR) technique combined with this layout technique, however, resulted in a massive 47% reduction in cross-talk induced delay!
A cross-talk estimation model has been developed for implementation in the B-RoCKIT tool. This model has the advantage (and was required for) quick estimation of the cross-talk induced delay impact with residing the need for time consuming and detailed SPICE simulations. The model has been verified to be accurate within 1% with respect to SPICE ignoring line-inductance, and within about 3% assuming a line-inductance of 1nH. The accurate and fast model allows the tool to quickly explore various design options and configurations to find the optimal solution.
We have found that the power-delay product of the MDR code applied to an 8-bit bus is 33% lower than for a standard Hamming code implementation, whereas the improvement for a 32 bit bus using MDR is still 16% better than a standard Hamming coded bus implemented on the same bus-footprint, despite the much larger number of wires for the MDR code!
3. Simultaneously Switching Output noise
We did not fully succeed in the development of a new code with inherent low switching activity. This is partly due to the limitation of the application of fault tolerant coding in the spatial domain (bits) and not in the time domain (serial encoding) since these would result in complex, hence power and area consuming codec-circuitry. Partly it is due to the fact that some coding mechanisms which have the potential of reducing the SSO noise require matching driver circuitry to fully exploit the benefits of the coding technique (e.g. to have a constant current drive matching with a N-out-M code). Nevertheless, by combining bus-invert coding with Hamming and (modified) dual rail coding in an efficient

way, we found a way to reduce the SSO noise by about 50% at the expense of reduced savings on power consumption and cross-talk.

Future work should especially be focussed on bus-driver design as we found the drivers to have a dominant influence on SSO noise. For optimal design, the driver design and coding method applied should be matched as to obtain the best results.

4. Unification of fault tolerant coding with respect to power, cross-talk and SSO noise reduction

We were able to optimise fault tolerant coding with respect to reducing cross-talk and power consumption. This resulted in the modified dual-rail code, which greatly outperforms Hamming codes (having less signal wires!) with respect to power-delay product and cross-talk, even though the bus-area (silicon cost) for the different methods is kept the same. For SSO noise, we found a way of reducing the switching activity on the bus, hence reducing the SSO noise up to 50%. The SSO noise reduction was incompatible with power/cross-talk reduction, and the importance of the noise with respect to power/cross-talk can not be decided by a tool. Therefore, the choice whether to implement reduced switching or not is left to the designer and we developed the prototype tool such that the designer is optimally supported in his decision. The designer has the knowledge of the power-grid design, the importance of the various criteria, and can easily take appropriate decision as the tool presents the results of various options in an integrated way. As the developed B-RoCKIT tool operates interactively and presents all the results in a consisting way, the unification of the coding approach is reflected in the final decisions of the designer. When the decisions is made, the tool will generate the hardware description for encoder, decoder (either with or without bus-invert coding) and a bus specification, ready for use with back-end IC design tools.

4. Dissemination and exploitation

The dissemination and exploitation are highly linked between the partners. E.g. many of the publications written by the university of Bologna are co-authored by project members from Philips and vice-versa. Therefore, the dissemination and exploitation activities are not separated per partner, but listed as an integral part, indicating the role of each partner where possible.

4.1 Dissemination activities

A significant amount of effort has been spend on dissemination throughout the project by means of articles presented on peer-reviewed conferences. These conferences not only allowed for spreading the obtained results and insight into the relevant scientific and industrial community, but also allowed for early feedback and input for our research. During the project, 3 papers have been presented on the IEEE International On-Line Testing Symposiums (IOLTS) (held within Europe), 1 paper on the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (held within the USA), 1 paper has been presented on the IEEE organized conference on Design, Automation, and Test in Europe (DATE'04) (held in Europe), and 1 paper will be presented later this year on the fourteenth International Workshop on Power and Timing Modelling, Optimisation and Simulation (PATMOS '04) (also held within Europe). In most of these publications, the University of Bologna had the leading role, though close cooperation with the other partners was indispensable and successful. 1 Journal paper has already been submitted to the IEEE Design & Test of Computers, and more journal papers are expected from the university of Bologna.

4.2 Exploitation activities

Apart from the use of the obtained knowledge and developed B-RoCKIT tool for future research and teaching at the university of Bologna, the exploitation and use of the project results is in the hands of both the industrial and small-emerging partners. During the project, the partners were using the prototype tool developed by iRoC within this project for obtaining the results on intermediate different bus configurations and provided early feedback on use, interfaces, bugs and suggestions for improvement. After the project, the iRoC will add this tool to their product portfolio of licensable products after further commercialisation and will be using this tool within their own design flow for fault tolerant systems. As they already had ways for the design of fault tolerant CPUs and memories, now they are able to eliminate the missing link by offering the fault tolerant bus design by means of the B-RoCKIT tool.

Philips will continue to use the developed prototype tool for a new research project on ultra-low power design. Due to the extreme demands on power in this project, supply voltages are scaled to a bare minimum, noise sensitivity (i.e. SSO noise) and data integrity are among the main issues being addressed and requiring a fault tolerant design. Next to these fault tolerant issues, there are parameter spread problems, and questions on real-time performance and adaptive processing. Furthermore, the knowledge gained on fault tolerant and robust design is finding its place in design flows focussed on soft-errors, allowing IC designs to withstand random errors caused by cosmic radiation (even at sea level!) in 65 nm IC technology and beyond.

Further details on dissemination and exploitation can be found in the dissemination and use plan, as implemented by the eTIP, as well as on the project website:

<http://www.extra.research.philips.com/euprojects/ft-ea/index.htm>

5. Project deliverables

Deliverable	Description	Delivery Month	Responsible partner	Status
D1	Optimal ECC for Power Consumption and Power-Delay Product Reduction, and Encoding/Decoding Circuitry for the Optimal ECC	May 2003	University of Bologna	Submitted month 7
D2a	Prototyping for Fault Tolerance, Power Consumption and Power-Delay Product Reduction	September 2003	University of Bologna	Submitted month 9
D2b	Description of the Prototype			
D3	Optimal ECC for Cross-talk Induced Peak Voltage Reduction and Encoding/Decoding Circuitry for the Optimal ECC	August 2003	Philips	Submitted month 8
D4a	Prototyping for Fault Tolerance and Cross-talk Induced Peak Voltage Reduction	December 2003	Philips	Submitted month 12
D4b	Description of the Prototype			
PPR1	Periodic Report covering the first 12 months	Jan 2004	Philips	Submitted month 13
D5	Optimal ECC for Simultaneously Switching Outputs and Encoding/Decoding Circuitry for the Optimal ECC	December 2003	Philips	Submitted month 14
D6a	Prototyping for Fault Tolerance and Simultaneously Switching Outputs	March 2004	Philips	Submitted month 14
D6b	Description of the Prototype			
D7	ECC for Combined Electrical Aspects and Encoding/Decoding Circuitry for the Optimal ECC	May 2004	University of Bologna	Submitted month 17
D8	Prototyping for Fault Tolerance and Combined Electrical Aspects	June 2004	University of Bologna	Submitted month 18

6. Conclusions

Our ambition with this project was to achieve a single coding/decoding scheme, which is capable of tackling not only the preliminary fault tolerance, but all important issues in bus communication. We did analyse the different electrical issues one by one to finally arrive at a complete insight and are able to offer an unified approach by means of the developed prototype fault tolerant bus-design tool. We have shown that power saving is feasible using new codes, and that the savings on power-delay product can be substantial. Furthermore, we have shown the ability to reduce the effects of cross-talk by more than 40% without increasing the area of the bus. Although not completely implemented in a unified way, we were able to offer a reduced switching fault-tolerant encoder/decoder solution, capable of reducing switching activity and corresponding (SSO) noise with almost 50%.

We expect that our new technology is essential for the design of reliable cost-performance electronic systems within 6 to 7 years from now. We expect that this new technology will hop in with safety critical devices first, and will find its way in regular consumer ICs thereafter.

Based on the results of this project, we foresee that significant improvements are feasible with an approach based on a combined mapping of data words onto a reduced switching fault detecting code with a matching electrical driver design. Unfortunately this was beyond the scope of this project.

7. Appendix: Published Papers

7.1 Conference Papers originating from FT-EA project

"Power Consumption of Fault Tolerant codes: the Active Elements",
D. Rossi, V.E.S. van Dijk, R.P. Kleihorst, A.K. Nieuwland and C. Metra,
Proceedings IEEE International On-Line Testing Symposium (IOLTS'03),
pp. 61-67, Kos, Greece, July 2003,

"Crosstalk Effect Minimization for Encoded Busses",
L. Di Silvio, D. Rossi, C. Metra,
Proceedings IEEE International On-Line Testing Symposium (IOLTS'03),
pp. 214-218, Kos, Greece, July 2003

"Error Correcting Codes for Crosstalk Effect Minimization",
D. Rossi, S. Cavallotti, C. Metra,
Proceedings of IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems
(DFT'03), pp. 257-264, Boston, MA, 3-5 November 2003

"Why Transition Coding for power minimization of On-Chip Buses does not work",
C. Kretzschmar, A.K. Nieuwland, D. Müller,
Design, Automation, and Test in Europe (DATE'04), pp. 512-517, Paris, France, February 2004,

"Impact of ECCs on Simultaneously Switching Output Noise for On-Chip Busses of High Reliability Systems",
D. Rossi, A. Muccio, A.K. Nieuwland, A. Katoch and C. Metra
Proceedings of International On-Line Testing Symposium (IOLTS'04), pp. 135-140, Madeira, Portugal, 12-14 July 2004.

"Reducing cross-talk induced power consumption and delay",
A.K. Nieuwland, A. Katoch and M. Meijer,
To appear in Proceedings of the fourteenth International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS '04), Santorini, Greece, 15-17 September 2004.

7.2 Journal papers originating from FT-EA project

"New ECC for Crosstalk Impact Minimization",
D. Rossi, A.K. Nieuwland, A. Katoch and C. Metra,
Submitted to Design & Test of Computers

7.3 Patent applications originating from FT-EA project

PHNL030972EPS

"Gating the correction signal in error correcting decoders to save energy",
R.P. Kleihorst, V.E.S. van Dijk, André K. Nieuwland, Filed September 2003

PHNL040225EPS

"AC/DC stable code"

R.P. Kleihorst, A.K. Nieuwland, V.E.S. van Dijk, C. Metra, Filed March 2004

PHNL040226EPS

"Reduced switching AC/DC stable code",

A.K. Nieuwland, Filed March 2004

"Fault tolerant bus coder with reduced switching noise and reduced delay",

A. Katoch, A.K. Nieuwland

(Patent application is currently being drafted)