	<p style="text-align: center;">FLASH</p> <p style="text-align: center;">IST-2001-38901</p> <p style="text-align: center;">Fundamental and Applications of Laser Processing for Highly Innovative MOS Technology</p>
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<h2>Final Report</h2>	
<p>Report Version: 3</p>	
<p>Report Preparation Date: February 16th, 2006</p>	
<p>Classification: INTERNAL</p>	
<p>Contract Start Date: JANUARY 1st, 2003 Duration: 36 months</p>	
<p>Project Co-ordinator: Vittorio Privitera</p>	
<p>Partners: CNR (Italy), ST (Italy), MicroLas (Germany), Uni Oslo (Norway), Lambda Physik (Germany)</p>	



**Project funded by the European
Community under the “Information
Society Technologies” Programme (1998-
2002)**

Executive summary.....	4
Project objectives.....	8
Methodologies.....	11
Project results and achievements.....	15
Deliverables and references.....	28
Future outlook.....	43

Executive summary

The sweeping progress in the field of nanoelectronics is claiming for annealing methods beyond the state of the art, in the millisecond range or even more rapid, to achieve the performances requested in the next decade, in terms of size and speed of the devices.

This was the lever rising the need of pursuing an innovative solution, that was the core activity of



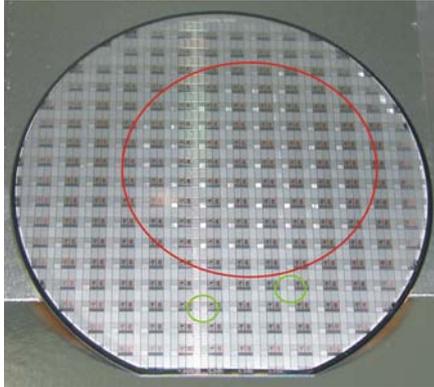
Laser and optics tools used in the project for irradiation of MOSFET wafers

the FLASH project. The approach we explored used excimer laser beams to heat silicon at very high temperatures, even above its melting point, for hundreds of nanoseconds. By this revolutionary method it would be possible to realize nanometer sized transistors, such as those with gate length of 32 nm indicated in the ITRS for the 2011 technology node.

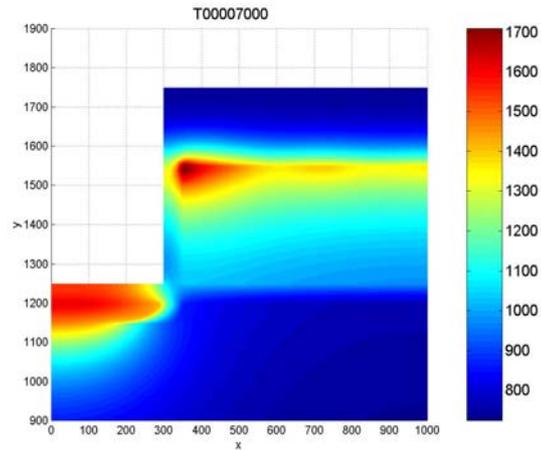
The consortium succeeded in achieving high performance transistors using Excimer Laser Annealing (ELA). Indeed, a full sequence production of transistor prototypes was started, by exploiting the scientific findings achieved by the Consortium. The main results of the project are contained in two patent proposals recently submitted and in fifteen scientific papers, published in high impact journals during the project period.

The integration of ELA into the MOS technology implied a noteworthy effort, because of the need of maintaining the integrity of the gate stack, while at the same time ensuring a perfect annealing of the source/drain junctions. We applied the processing methods developed within the frame of the project, as well as rode on a wave of increasing enthusiasm, based on the encouraging electrical results of the first fabricated transistors, to develop novel device structures using dielectric mirrors or double polysilicon layers, in order to shield the gate electrode from the laser radiation.

While comprehensive investigations, involving structural and morphological imaging at high



Device wafer treated by excimer laser annealing. The circle indicates an area irradiated by laser.



Thermal field induced by ELA in the cross section of a device structure, as simulated by the software CLASS developed within the frame of the FLASH project.

magnification and resolution as well as electrical and chemical characterization, were undertaken to evaluate the process reliability, also the statistical aspects of the device performance assumed a fundamental role, being a device production pursued. Therefore, both single structures and transistors were evaluated and statistical analysis of the device wafers was performed. A process window, suitable for industrial purposes, was accomplished exhibiting a device yield higher than 90% on wafer.

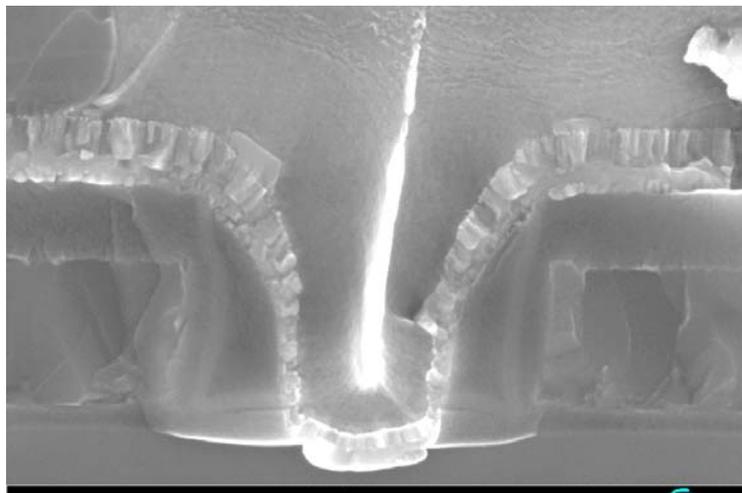
The experimental activity has been massively sustained by modelling and simulation. The software CLASS (Catania Laser Annealing Simulation Suite), developed by the consortium, has been conclusively calibrated and evaluated, and it is now a reality in the field of process simulation.

The clear objective of this project was the integration of laser processing into the MOS technology; for this purpose we have used the low voltage MOS technology. The device structures we have used, as well as the process flow where the ELA process was integrated, belong to such class of MOSFETs. For this activity the consortium succeeded: the laser based process has been integrated and prototype devices have been realized. Moreover, these results lay the foundations for a further enterprise, i.e. to apply this process to ULSI, where it might have even a greater impact. In fact, we have demonstrated that Laser Thermal Processing in the melting regime can be used for junction fabrication in real devices, producing reliable electrical performances; melting areas of the device is hence not necessarily a drawback impeding the application of ELA, but a phenomenon that can be controlled and taken advantage of, under specific conditions relative to the device structure and the process. In conclusion, the FLASH project has opened a new frontier in the area of innovative processing for future silicon devices, as well as given an impulse to a new market segment for laser technology.

The successful exploitation of the project results was achieved by the application of the findings on excimer laser annealing to the industrial processes commercialized by MicroLas. Moreover, the results relative to the processing and materials characterization will be made available to the microelectronics industry taking part to the project, i.e. ST.

Another goal of the project was the release of a process simulation program for the excimer laser annealing methodology. This simulation program is available to the two companies present among the participants, with both an impact on processing (MicroLas) and design of new devices (ST). Furthermore, the developed software can be now released to any institution in the micro/nano electronics field, and based on the adequate dissemination made by the consortium, the software may become a widespread product.

The results of FLASH further advanced the know-how of MicroLas in the field of annealing methods and in this way further improved the market position of the company. The main objective of MicroLas is to keep a strategic position as a supplier to the international microelectronics industry and in the market of innovative tools. At the same time ST might expand its device portfolio by implementing the laser annealing process into the fabrication of MOSFET, so producing new generation devices with extreme performances. The results of the FLASH project will be disseminated and commercialised around the world using the existing marketing organisation of ST.



SEM Cross section of the ELA-MOSFET .

The consortium was formed by specialists in solid-state physics, materials science and electronic engineering, with extensive experience in analytical techniques and advanced processing of silicon devices as well as mathematical modelling and computer simulation. By a unique combination of these features, basic physical issues on defects, dopant diffusion and electrical activation, related to

the excimer laser annealing process, were addressed. The consortium aimed to achieve fundamental results that will have an application in the industrial processing of semiconductor devices.

The partners in the consortium were carefully selected in order to ensure that the expertise available in Europe could be successfully used to organise and carry out a research project on electronic device processing development. The consortium was formed by the strategic alliance of five partners. Due to its long lasting experience in ion implantation, device processing, characterisation techniques and process simulation, CNR-IMM was chosen to coordinate the FLASH proposal. At CNR-IMM, high expertise in computational methods is available, ranging from atomistic molecular dynamics to large-scale Monte Carlo and continuum models; this knowledge greatly contributed to modelling and simulating the interaction of the laser beam with a device structure. Moreover, CNR-IMM is internationally known as one of the excellence centres for ion implantation studies and has solid traditions in the related structural characterisation techniques.

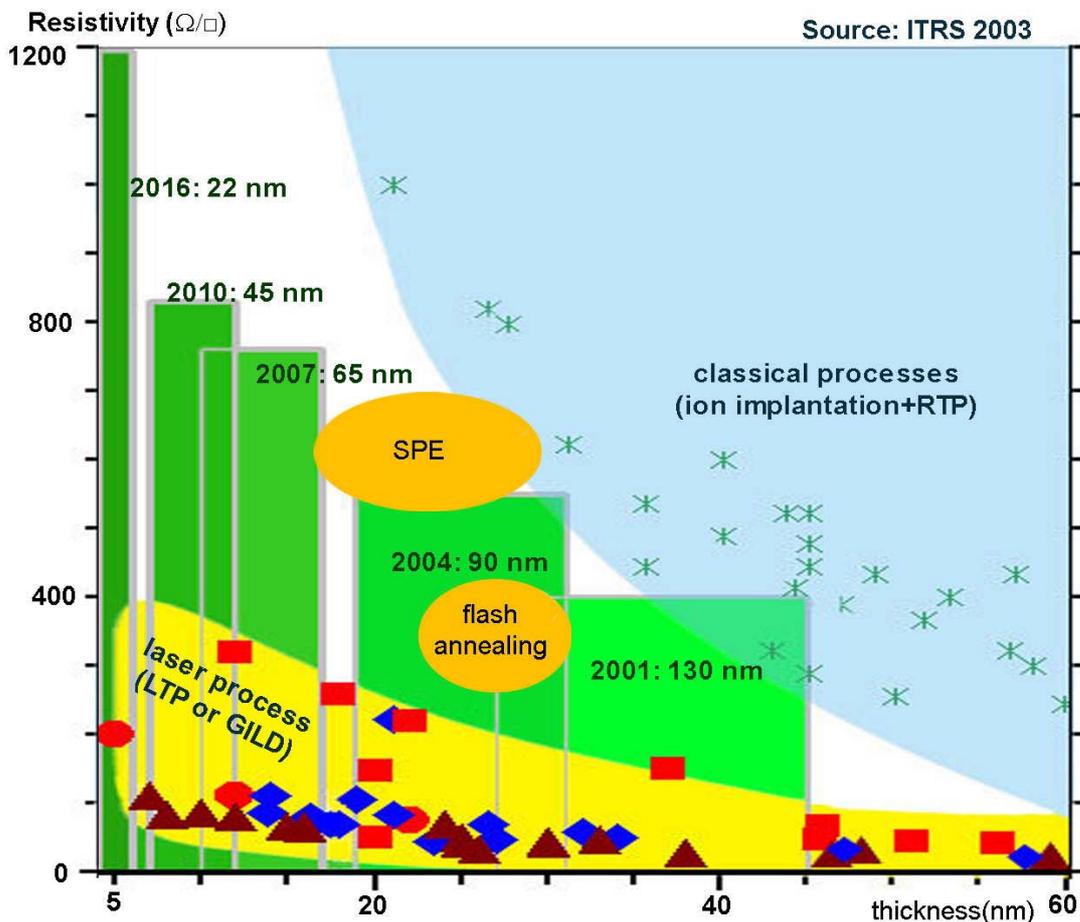
The other research partners in the FLASH project have been selected due to their specific expertise in the required fields of semiconductor physics and materials analysis. CNR-IFN is one of the leading groups in Europe in the area of laser physics and its applications; this institution gave also the possibility of a flexible research clean room for special experiments. The group at the University of Oslo has a long lasting experience in chemical and electrical characterisation of materials and devices. Moreover, this group significantly contributed to the research work through its expertise in the ion implantation and related damage field.

In order to assure the exploitation of the project results to the European industry, the German company MicroLas was involved to provide laser and optics equipment with suitable throughput for industrial device applications. MicroLas was one of the leading equipment suppliers in terms of application of excimer lasers and other UV lasers, commercialisation and support of the most advanced products for laser processing. MicroLas, as a subsidiary of Lambda Physik, the world leader company in excimer laser, was thus the ideal partner to develop innovative tools able to ensure an industrial exploitation of the project findings. At project mid-term, MicroLas was fully adsorbed by Lambda Physik, that became an official project partner.

Finally, ST-Microelectronics, as one of the most important microelectronics companies in Europe, offered the most recent technology for MOSFET fabrication. The large facilities of ST were used to evaluate the real feasibility of laser processing in an industrial environment. Moreover, within the consortium this company represented the final user of the “know-how” collected during the project.

Project objectives

The semiconductors industry and its suppliers are the cornerstone of today's high-tech economy. Representing a worldwide sales value of 250 billion euro in 2004, the sector supported a global market of more than 6 trillion euro in terms of electronic systems and services, with applications ranging from transportation to health care, and from general broadcasting to electronic banking. Semiconductors have pervaded our lives in the past fifty years. The shift from the past era of microelectronics, where semiconductor devices were measured in microns to the new era of nanoelectronics where they shrink to dimensions measured in nanometers, will make the semiconductor sector even more pervasive than it is today. The new era of nanoelectronics will give



Junction depth and sheet resistance requirements according to the ITRS 2003 for the CMOS technology nodes.

next-generation products that will elevate the ICT (Information and Communication Technology) society to unprecedented levels and it will enable Europe to realize its vision of Ambient Intelligence – living environments that are aware of our presence and responsive to our needs.

Innovative solutions are hence needed for the major device, process and material integration challenges, anticipating the nanoelectronics technologies planned for industrialisation in the next 8-12 years.

However, in order to achieve the technology nodes below 65 nm, many issues have to be tackled, such as short channel effect (SCE), gate leakage and mobility degradation, and simple scaling down without proper optimisation based on experiments and simulation become worthless. Moreover, several device parameters are approaching their physical or technical limits: gate oxide thickness, source/drain junction depth and parasitic resistance, including contact and wiring resistances. This means the end of the conventional scaling scheme and the beginning of a new one. In order to further improve the VLSI performances, we need equivalent scaling by means of the introduction of new materials and/or new processes.

In this project we devoted our efforts mainly to the doping issues. Sub-90 nm MOSFET architecture needs ultra-shallow junctions and 2D dopant profiles design to control the SCE and the sub-threshold performances. Indeed, the formation of ultra-shallow source-drain extensions with high doping level and an optimal dopant distribution in the channel zone allows one to reduce the parasitic effect of threshold voltage roll-off versus channel length decrease. It is well known that the fabrication of such ultra-shallow p^+/n junctions is one of the main challenges for the production of sub-65 nm pMOSFET. Apart from the junction depth and the high doping level, also an extreme lateral abruptness of 2.5 nm/decade is required, in order to decrease the spreading resistance, and hence the total resistance, of the current path in the MOS circuit. The requirements for current CMOS have been met by the use of ion implantation with energies below 1 keV and the so-called “spike annealing” technique. The latter gives the possibility of extremely fast ramp rates, > 250 °C/s, and a soak annealing time that is close to zero. Nevertheless, the junction depth, the electrical activation and the profile abruptness achievable by this process are not suitable for the future generation technology nodes.

The alternative proposed by this project was represented by the use of excimer laser annealing for the formation of ultra-shallow abrupt junctions with high electrical activation. This technique appeared quite promising, but exhibited severe technology integration issues. The aim of this project was hence to provide the physical assessments (both theoretical and experimental) needed to support the application of the excimer laser annealing (ELA) method to the future CMOS technology.

Potentially, this method is very attractive to meet the requirements of the future technology nodes. In the ITRS, many items are indicated by red, when the technology node is less than 100 nm. Critical items include gate stack, junction depth, sheet resistance at contact and extension, power

dissipation and cost effective integration. The ELA method can certainly contribute to break the “red brick wall” present in the roadmap, but a major issue related to the ELA method remained its integration with the process steps and the materials used for the device fabrication. An intense activity was hence devoted by this consortium to the study of the interaction of the laser beam both with doped silicon and with the structures forming the device, like dielectrics, metal contacts and polycrystalline silicon. Therefore, the doped layers were studied in one and two dimensions, by state of the art analytical techniques, to obtain data also on the lateral diffusion of the doping impurities beneath a mask. A process flow, aimed to the realization of a MOS device, compatible with the inclusion of ELA process was finally elaborated and implemented.

Furthermore, reliable computational packages, for TCAD groups developing processes for the future CMOS technology, was produced by the consortium. We planned to search for reliable computation solutions, to be coupled and integrated with existing codes for process simulation, capable of simulating the interaction between the laser beam and the silicon device, including the evolution of the thermal field and dopant distribution during ELA and the subsequent quenching. The FLASH project had therefore two inter-related specific objectives: : i) the realization of packaged transistors treated by ELA and their electrical testing ii) the release of the simulation software describing the interaction in two dimensions between the laser beam and the MOSFET. These objectives were achieved, in line with the scheduled activity, also based on the successful choice of the process conditions guided by industrial specifications provided by the industrial FLASH partners, using their experience with the demands of the semiconductor industry.

The consortium indeed achieved the two objectives indicated in the work plan, but this result was not considered by the partners as an ultimate breakthrough in the scenario of the innovative semiconductor devices. The reason was a simple marketing consideration: a demonstration of the process reliability will not convince the semiconductor industry to replace some of their processing steps with the ones assessed by the project, but attracting differences with respect to conventional annealing should emerge from the electrical testing, if an economic impact of the scientific findings is wished. With this aim the consortium also started the production of device wafers with a reduced channel length.

Further, device wafers were also produced with a multi layer, formed by SiO_2 and Si_3N_4 films, on top of the gate electrode to shield the latter from the laser radiation, so completely avoiding melting of polycrystalline silicon. This final experiment provides an additional solution eventually of crucial importance for further device technologies where ELA might be applied.

Methodologies

The approach to the project objectives was pursued through a careful analysis of the state of the art and the inherent limitations to the currently proposed methods. The methodologies employed in this project rely on the Si melting regime induced by excimer laser, that represented the core of this activity. The reason for such choice mainly lies in the possibility to obtain extremely sharp doping profiles, in terms of depth and abruptness, with high electrical activation, and to suppress the lateral diffusion of the dopant, with consequent advantages for the reduction of the short channel effects and the size scaling. This choice implies hard challenges to tackle, relatively to device integration, but promises to establish a real advantage with respect to the other annealing methods, even the ultra rapid ones recently proposed, with significant impact on the achievement of the future technology nodes. The feasibility and reliability of this process was tested through the application to low voltage MOSFET. Even though the semiconductor players are more concerned with the application of new methods to the CMOS technology, the use of such innovative annealing in the power field can open new perspectives for the VLSI power devices, that definitely need suitable thermal processing as well. On the other hand, testing ELA on larger MOS structures does not, by any means, exclude its extension to ULSI, by exploiting opportune solutions, relatively to the structure and the process itself, as it was demonstrated by the project results. Anyhow, all of these considerations were analysed in comparison with the activities and the results of other groups active in this field.

Three main ‘sources’ have been used by the consortium to evaluate the current state of the art in the field of advanced thermal processing for semiconductor devices: the Workshop organized by CNR-IFN in Roma, January 2005, entitled “Non-conventional thermal processes for advanced CMOS”; the critical analysis of recent patents in the field of laser annealing for thermal treatments of semiconductor devices; the 13th IEEE International Conference on Advanced Thermal Processing of Semiconductors (RTP 2005).

The general message coming out from the Workshop is that alternative annealing techniques are definitely needed for the next technology nodes. If they are to be based on lamp illumination or laser radiation is a matter of ‘temerity’ by the approach that is pursued; Flash Lamp Annealing and/or Non Melting LTP, with ultra violet or infra red sources, are an extension of the by now surpassed Rapid Thermal Annealing method, whereas the use of melting ELA requires a noteworthy effort of integration, but provides doping profiles with unique characteristics.

That RTA is surpassed, was also the general message launched at the 13th IEEE International Conference on Advanced Thermal Processing of Semiconductors (RTP 2005), held in Santa

Barbara (USA) in October 2005. Concerning the advancements made in the field of FLASH, an important forum was represented by this conference, collecting the most recent highlights published worldwide. The focus of the conference, relatively to the junction formation, was mainly on the use of Flash lamp assisted RTP and Laser processing for keeping up with the Moore's Law. The talks in the Laser Processing Session pointed out that, while keeping paced with the Moore's Law has been so far accomplished by decreasing processing times, fundamental limits are now projected for the 45 nm node, which requires processing time significantly shorter than those available by RTP, on the order of 10 ms or even less and with nearly zero diffusion. This is beyond the processing regime currently provided by lamp based RTP systems, which are instead limited to processing time on the order of 1 s. In order to meet this new processing requirement, major semiconductor industry suppliers have identified Laser Annealing as one of the process solutions to enable ultra shallow junction formation for the 45 nm technology node; as an example, a group formed by IMEC and Applied Materials presented at this conference the formation of ultra shallow junctions by a sub-melt laser annealing process based on diode laser operating at the wavelength 810 nm. This group concluded that laser annealing is an attractive candidate for fabrication of device nodes below 65 nm, dramatically improving sheet resistance with minimal diffusion, which should translate into improved device performances. The results shown are comparable with those obtained by the FLASH consortium at the end of the first project year, no level of integration is reported by these authors yet.

Some recent patents, relative to methods for fabricating transistor by laser annealing, have been identified. All of them report as assignee one of the world leading edge semiconductor companies, Advanced Micro Devices (AMD) from Sunnyvale (USA).

The patent by Yu et al. (6,902,966 USA June 7, 2005), entitled "Low temperature post dopant activation process", is focussed on the problem of dopant deactivation, as a result of high temperature post-dopant activation processes, such as rapid thermal annealing. Solving this issue is based on the activation of source/drain regions using laser thermal annealing, followed by a low temperature silicide formation process. In particular, nickel silicide is formed over the activated source/drain region by applying a nickel layer on the source/drain region and furnace annealing at low temperature. The temperature is sufficiently high to produce nickel silicide, that forms already at 400-500 °C, but sufficiently low to minimize dopant deactivation within the source/drain regions. In our experiments the deactivation following post-laser thermal processing was not an issue. We have studied the phenomena occurring during post-laser thermal treatments, in terms of atomic transport and electrical activation; the results showed that no significant deactivation takes place for our conditions. Indeed, it is known from the literature that such lack of electrical activation happens

in the case of extremely high implant dose, higher than $5 \times 10^{15}/\text{cm}^2$, not necessary, according to our experiments, to achieve sheet resistance values around 200-300 Ohm, well suited for source/drain applications.

Another patent by Paton et al. (6,867,080 USA, March 15, 2005), “Polysilicon tilting to prevent geometry effects during laser thermal annealing”, concerns the use of dummy structures for eliminating uneven melting of active areas of the device during laser thermal annealing. Indeed, conventional methodologies for performing laser thermal annealing result in uneven heating of the semiconductor substrate when the surface feature density varies. This patent solves such problems stemming from conventional manufacturing processes. In particular, uneven heating of active areas due to variations in gate electrode density is eliminated by adding dummy structures, formed simultaneously with the gate electrodes, to fill the spaces between isolated gate electrodes. In this way, the spacing between the gate electrodes and the dummy structures is the same as the spacing between the densest array of device structures on the substrate surface. Since the surface features, i.e. the gate electrodes and the dummy structures, appear essentially uniform to the LTA process, the laser radiation is uniformly absorbed by the substrate and the substrate surface is evenly heated. The patent refers to the melting regime, although the invention is not limited to this application.

Actually, in our conditions, we do not have to tackle variations in gate electrode density, however the invention seems interesting, regarding the issues raised during the experimental activity of the consortium. In fact, we have observed an important role of the thermal gradient in the bulk, causing for example the formation of incomplete re-growth, with the consequent formation of crystalline defects at the edge of the implanted source region. The use of dummy structures might eliminate such effects; the limitation seen by the consortium concerns, however, the removal of such sacrificial structures, for continuing the fabrication flow with subsequent spacer formation and metallization.

A further patent, entitled “Reduced dopant deactivation of source/drain extensions using laser thermal annealing” by Xiang et al. (6,812,106 USA, November 2, 2004), is closely related to both the two described above. It concerns the reduction of dopant deactivation of source/drain extensions during silicidation, by forming deep source/drain regions using a disposable dummy gate as a mask, forming metal silicide layers on the deep source/drain regions, removing the dummy gate and then forming the source/drain extensions using laser thermal annealing. The embodiments of this patent include angular ion implantation, after removing the dummy gate, to form spaced apart pre-amorphized regions, ion implanting to form source/drain extensions and then laser thermal annealing to activate the source/drain extensions. Subsequent processing includes forming sidewall spacers, a gate dielectric layer and then the gate electrode.

The proposed process flow is rather complex, based on the need to avoid dopant deactivation. Indeed, in our experiments we have not evidenced the necessity of using high implant dose to achieve optimal sheet resistance values. Indeed, the recent literature (“Thermal stability of dopants in laser annealed silicon”, Takamura et al., J. Appl. Phys. 92, 230 (2002)) reports deactivation effects for As dose above $8 \times 10^{15}/\text{cm}^2$ and B dose above $1 \times 10^{16}/\text{cm}^2$, in the implant energy range 10-40 keV, close to the one in which we operated. The implant dose we have used for As, applied to the transistor, as well as for B and BF_2 , used for diffusion and activation experiments, is definitely lower than those investigated in this article. In fact, no deactivation has been detected in our experiments and, hence, no need to use complex processing procedures as those reported in the above mentioned patent.

A signal of interest is represented by the rich production of patents by a leading company such as AMD. We noticed that a consistent activity on the use of laser processing for the semiconductor industry is performed in USA, where both semiconductor industry and equipment suppliers are quite active in this field. The activity in Europe is rather intense in academic research as well as among equipment suppliers, whereas the involvement of the semiconductor industry seems less heavy than in USA. In this context, the FLASH project has attracted European industrial interest towards new concepts of thermal processing, showing the applicability and reliability of laser annealing.

Project results and achievements

Comparison to the original project objectives

DOPING BY ELA

In Fig. 1, a schematic of the MOS structure used in our experiments is shown. The source regions are implanted with As and laser annealing was applied to activate the doped regions. In order to improve the coupling of laser radiation with the source regions, an oxide film was deposited, such that the reflectivity at 308 nm of the source region was reduced by the antireflective action of the

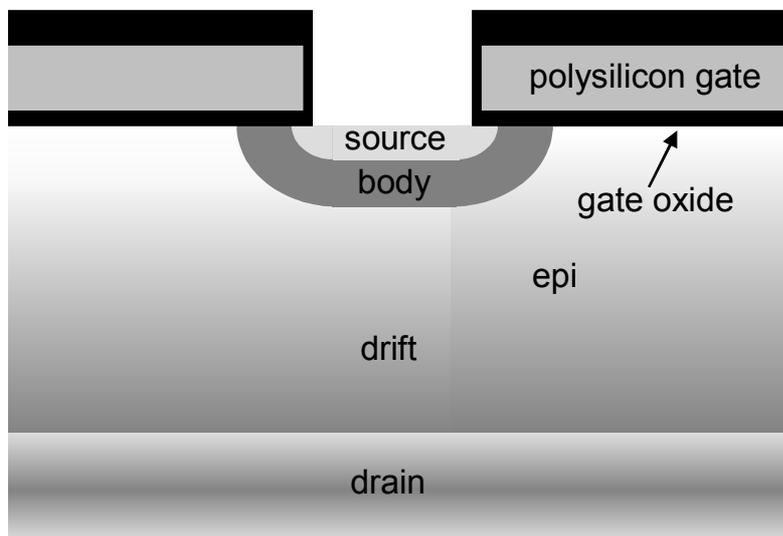


Fig.2 Schematic of the MOS structure used for the experiments.

oxide layer. The same oxide layer also covers the gate stack side walls, thus protecting the structure from mechanical deformations related to melting of the polysilicon gate. A cross-section Transmission Electron Microscopy (TEM) micrograph of the structure prior irradiation is shown in Fig. 2. The amorphous layer generated by the As implant is visible in the silicon region in between

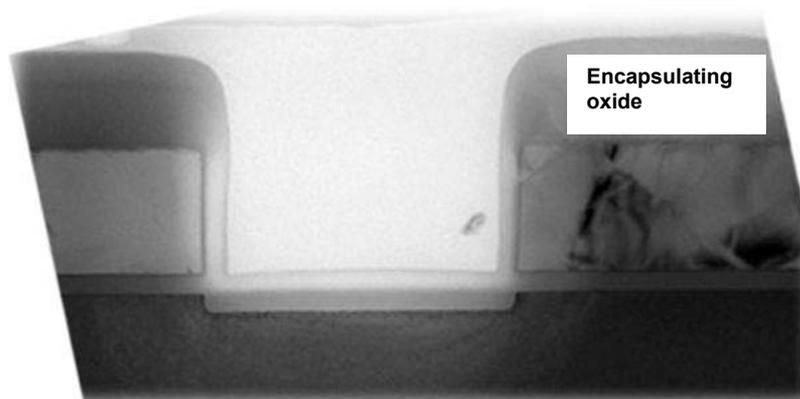
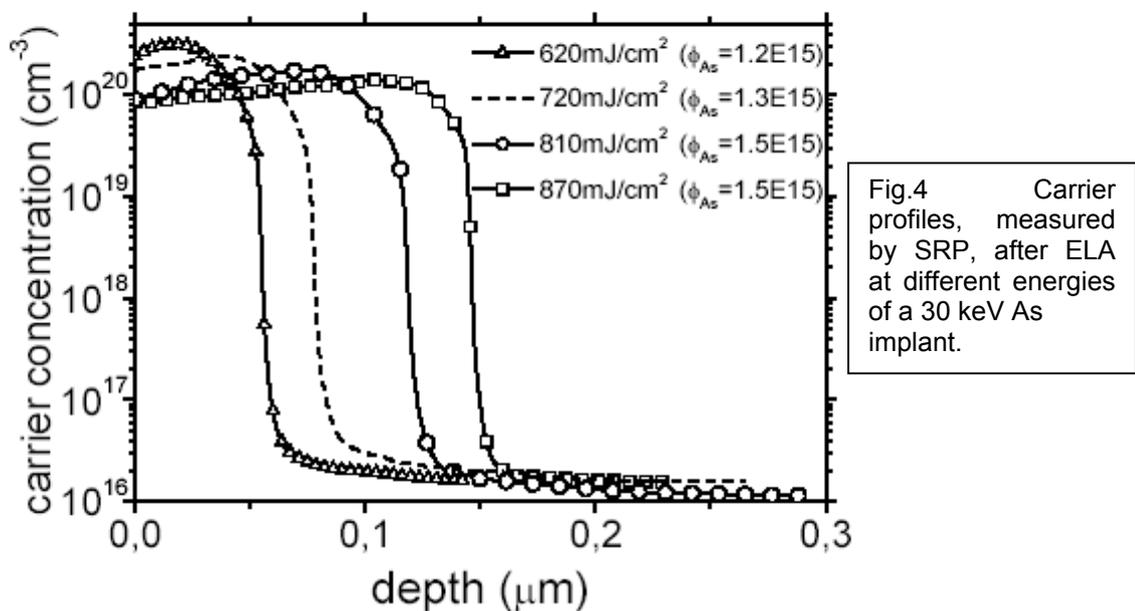


Fig.2 Cross sectional TEM of the fabricated structure.

the polycrystalline silicon stripes.

The laser apparatus used for irradiation was a Lambda Physik LPX 205 XeCl excimer laser (308 nm emitted wavelength, 30 ns pulse duration), delivering an homogeneous beam, with a variable spot size, that for our experiments was adapted to the chip size ($2.5 \times 3.5 \text{ mm}^2$), and with an energy density (E_d) that can be continuously changed, by using a beam attenuator, in the range 100-1200 J/cm^2 .

An example of the carrier profiles as a function of depth, associated to the As doping after ELA, is reported in Fig.3; they show a box-like shape with a very high abruptness of 2.6 nm/dec. Due to the extremely high diffusivity of dopants in liquid Si, the As atoms are able to redistribute almost



uniformly within the melted layer, up to the interface between the solid and liquid Si. The following rapid re-crystallisation from the liquid phase enhances dopant trapping and produces high electrical activation. The highest carrier concentration is achieved following shallow melting (620 mJ/cm^2) with a sheet resistance of $75 \Omega/\square$. Due to lateral heat dissipation occurring in the structured wafers, the junction depths obtained in such non patterned wafers can be rather different from the real device case. However, the one dimensional analysis of doping obtained by laser annealing is useful to determine the shape of the dopant profiles and their evolution with the irradiation conditions.

While annealing the source layer, the remaining part of the doped layers composing the MOSFET, such as the Boron doped body, is not altered at all by the laser irradiation. This is due to the short duration of the process, of the order of tens of nanoseconds, as well as to the fast dissipation of the heat through the Si substrate, determining a thermal process in solid phase of the underlying doped layers that lasts a few milliseconds, inducing a negligible diffusion not detectable by the analytical techniques.

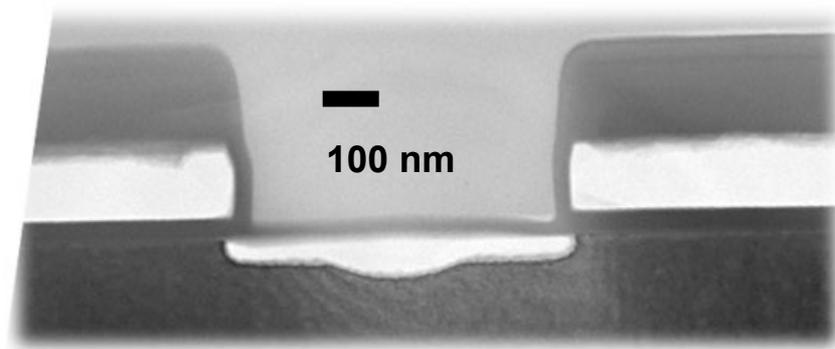


Fig.5 MOSFET cross sections observed by TEM. Selective chemical etch exhibits the source (white region) region obtained by ELA of a 10 keV As implant.

In order to preserve the gate integrity from the morphologic modifications induced by the laser irradiation process, an oxide layer surrounding the polycrystalline silicon gate electrode was employed. The integrity of the complete device structure after laser irradiation is shown by the cross section TEM analysis in Fig.5, where the two dimensional contour line of the doped region is identified by the white area in the implanted window; a deeper melting occurs in the central region

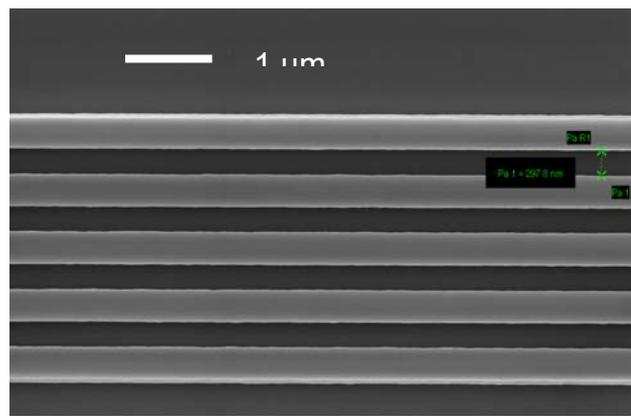


Fig.6 SEM image of polycrystalline silicon gate stripes after ELA

of the implanted window, due to lateral heat loss and to the diffraction of the laser light through the narrow geometries of the patterned sample. The lateral diffusion underneath the gate oxide is negligible, so providing the possibility to shrink the channel length without incurring in short channel effects.

The realization of a device implies the reliability of processing and patterning over a large scale, in order to ensure a high yield, necessary for a real industrialization of the method under investigation. A SEM image of a MOSFET chip irradiated by laser is shown in Fig.6, attesting the integrity of the structure subjected to ELA when operating under optimised conditions.

TWO-DIMENSIONAL NUMERICAL MODELING

A phase field methodology was preferred to conventional methods to model the dopant evolution during melting. Standard modelling is based on the numerical solution of the heat diffusion and on a step-like change of the mass transport properties across the solid/liquid interface, while an ‘ad-hoc’ segregation model rules the gap in density across the interface itself. In this sharp interface model, the thermal and mass transport are de-coupled and the segregation coefficient at the interface can be included by fitting the experimental results. For the numerical calculations an obvious drawback of

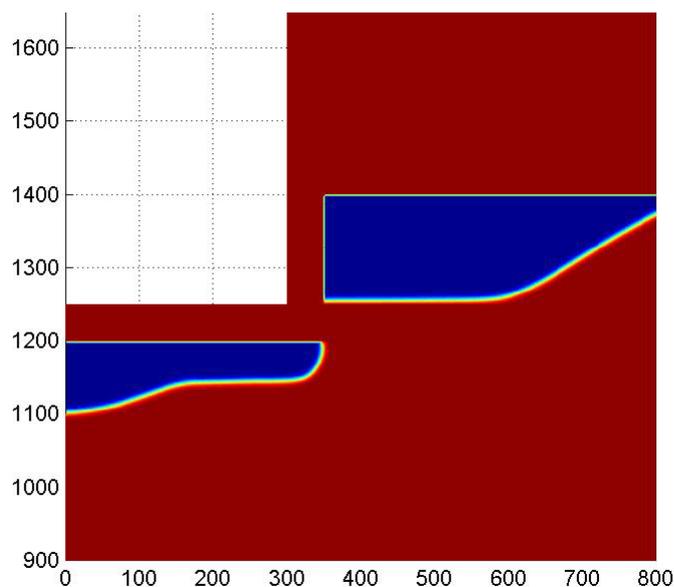


Fig.7 Two dimensional simulation of melting following laser irradiation, as obtained by the phase field calculation.

this methodology is that the instantaneous interface position and speed should be found. This poses some limitations, especially for its application in 2D calculations or when the whole device structure has to be considered.

The phase-field methodology is instead based on a physical description of the moving phase boundary problem considering a finite dimension of the transition region between the two phases. Tracking the boundary location is not necessary for the numerical simulations since phase, temperature and dopant density evolve concurrently according to the three coupled differential equations:

$$\frac{\partial \Phi}{\partial t} = -(\mu / 6l) \frac{\delta F}{\delta \Phi} = (\mu / 6l) \left[\varepsilon^2 \nabla^2 \Phi - \frac{\partial f}{\partial \Phi} \right]$$

$$\frac{\partial c}{\partial t} = \vec{\nabla} \left[(v_m D(\Phi) / RT) c(1-c) \vec{\nabla} \frac{\partial f}{\partial c} \right]$$

$$\rho c_v \frac{\partial T}{\partial t} + 6\Phi(1-\Phi)[(1-c)L_{Si} + cL_X] \frac{\partial \Phi}{\partial t} = \vec{\nabla} \left[K(\Phi) \vec{\nabla} T \right] + S_{laser}(r, t)$$

where Φ is the phase, F the free energy, f the potential term, C the dopant concentration, T the temperature and S the light source intensity.

The phase field method, based on the Ginsberg-Landau approach to the phase transition problem, was then applied to the simulation of thermal field evolution and dopant redistribution during ELA of implanted samples.

The requirements of an efficient simulation imposed structural changes in the code for two dimensional structures, such as the space discrete approximation and the method for time integration. In addition, the heat source was numerically evaluated, simulating the interaction between the laser electromagnetic wave and the patterned surface of the Si wafer, by means of the finite difference time domain (FDTD) approach, based on the numerical solution of the Maxwell equations.

Such modeling approach allows one to quantify the dependence of the junction depth on the position in the implanted window. Fig. 7 illustrates a simulated dopant distribution, referring to the experimental case of Fig.4. The blue colour represents melting, that in turn means homogeneously redistributed As. All the main features of the resulting doping distribution after ELA are perfectly reproduced by the model, with a deeper doping profile in the center of the window, resulting from the combined effects of lateral heat diffusion and diffraction effects. This simulation code not only yielded a precise interpretation of the experimental results but also enabled a predictive analysis of different gate stack architectures and geometries and the optimization the ELA conditions.

INTEGRATION IN MOS TECHNOLOGY: FABRICATION OF TRANSISTORS

MOSFET wafers were fabricated according to the structure described in Fig. 3, based on a process

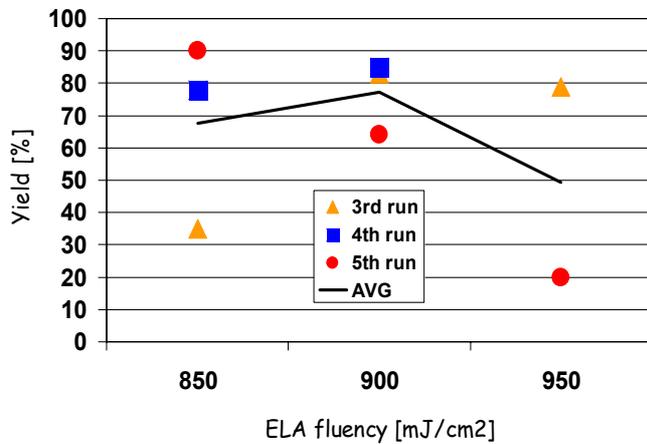


Fig.8 MOSFET yield versus oxidation thickness of eventual fractures in the encapsulating oxide, caused by melting of the polycrystalline silicon gate electrode.

flow defined according to the indications coming from the experiments and the modelling and simulation work. The laser annealing process has been realized by a mask projection tool in order to irradiate a single device with a uniform laser beam, avoiding beam tails. The MOSFET yield versus ELA fluence, for the transistors with optimized structure and treated with the most reliable processes, is reported in Fig.8 for three lots of wafers. Both at 850 and 950 mJ/cm² a large yield spread is observed for the three lots, whereas the 900 mJ/cm² group is more stable with an average yield of about 77%. The spread is due to the non proper processing, as the wafers traveled from one site to another – geographically distinct – site, exploiting the resources of different partners. Many dust particles can affect the device yield of these wafers, however, surprisingly high yield is still obtained, proving the robustness of the process.

Based on the evaluation of the best yield, as well as on process refinements, ELA-MOSFETs were fabricated, whose main characteristics are reported in Fig.9. The ELA processed devices have a threshold voltage comparable with the conventionally processed device and, if driven at 10 V, the

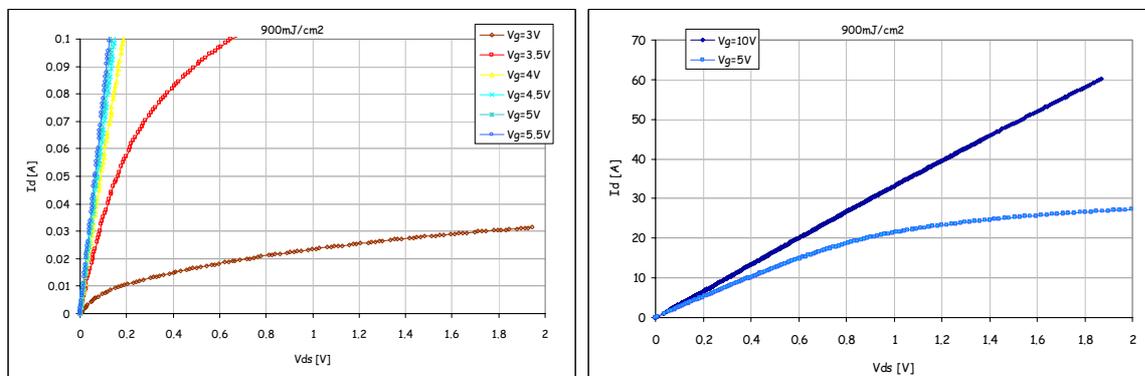


Fig.9 ON state characteristics for low (left side) and high (right panel) current.

MOSFETs are completely switched on and the ON resistance is comparable with the standard one. Such transistors were fabricated with a yield of $\sim 80\%$.

The reliability of the process was therefore demonstrated; the final aim was to prove that even superior electrical performances could be achieved by means of the ELA process. In particular, the potential of the ELA process as a “zero lateral diffusion” thermal treatment was worth exploiting. Hence, a set of MOSFET wafers was prepared, with a shallower body layer and a shorter channel, aiming to a lower ON resistance. The “on” characteristics are shown in fig.10 for the $900\text{mJ}/\text{cm}^2$ case. Thanks to the reduction of the channel length and of the JFET component between adjacent body wells, made possible by the use of ELA, that ensures zero lateral diffusion, a 10% decrease of the ON resistance of the transistor was obtained at high current. This is a clear advantage of using ELA, revealing itself as a suitable process to scale the channel length.

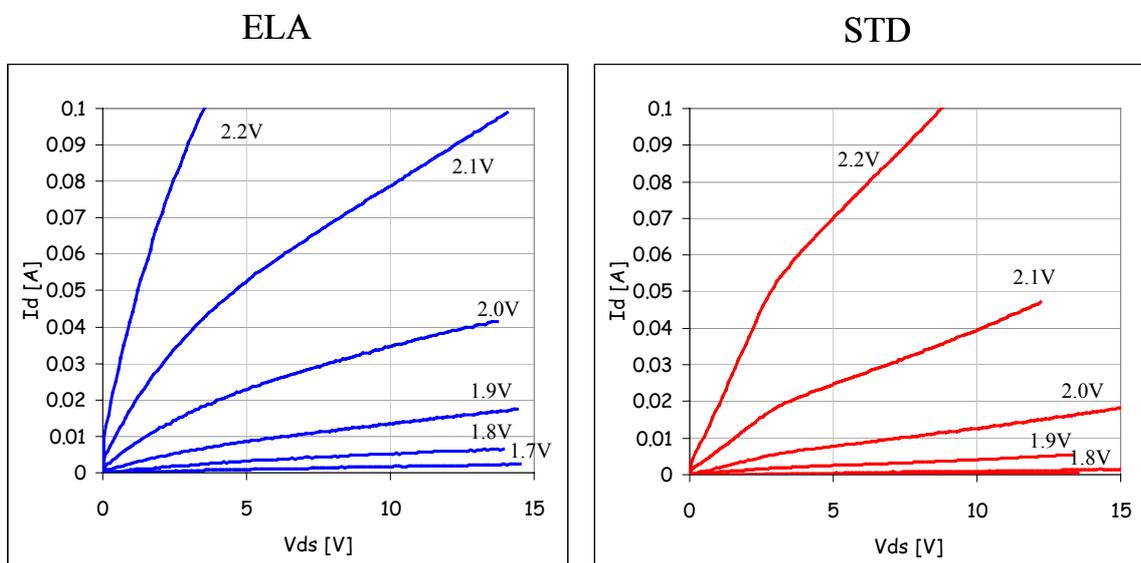


Fig.10 Drain current increase for the ELA treated MOSFET, with respect to the device processed by conventional thermal processing. An significant increase at low current levels is clearly evidenced.

Even though a satisfactory degree of reliability of the ELA MOSFET was accomplished, further efforts were pursued in order to design a new gate-stack structure, which could simplify the device fabrication. A new concept was proposed, where the gate stack is protected by a multilayer mirror optimized at 308 nm, fabricated on top of the poly-gate.

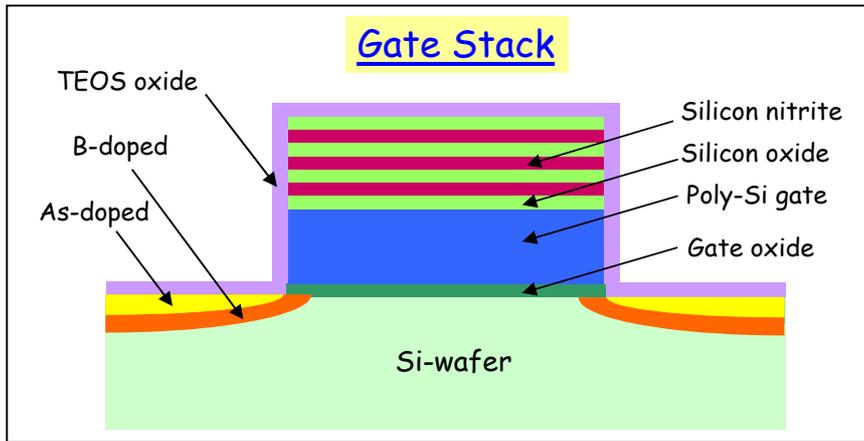


Fig. 11 Gate stack structure with dielectric mirror.

The dielectric mirror (Bragg reflector) consists of identical alternating layers of high and low refractive index, n_h and n_l , with optical thickness equal to quarter wavelength: $n_h d_h = n_l d_l = 308 \text{ nm}/4$. It should be also pointed out that the dielectric mirror was designed using SiO_2 and Si_3N_4 layers, as these are compatible with IC processing.

In Fig. 11, a dielectric mirror formed of a sequence of 6 layers is shown, including an additional 100 nm SiO_2 layer deposited on top of the dielectric mirror structure itself, the latter not altering the dielectric mirror reflectivity (being the optical thickness of this layer, $n_l \cdot d$, equal to $308 \text{ nm}/2$),

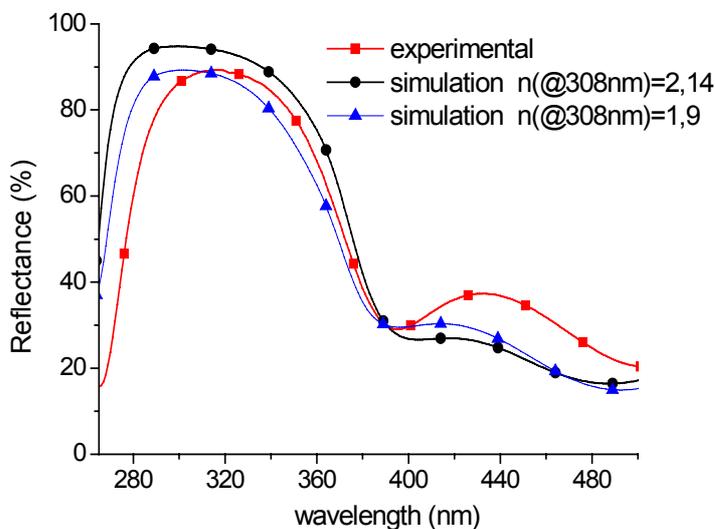


Fig. 12 Experimental and simulated reflectivity of a dielectric mirror, including 6 alternating layers of SiO_2 and Si_3N_4 and a final 100 nm thick SiO_2 layer.

In Fig. 12 the measured reflectivity is compared with simulations using two different values for the Si_3N_4 refractive index. In order to reproduce the measured data, a refractive index value of 1.9 is required, in agreement with that measured for PECVD deposited Si_3N_4 .

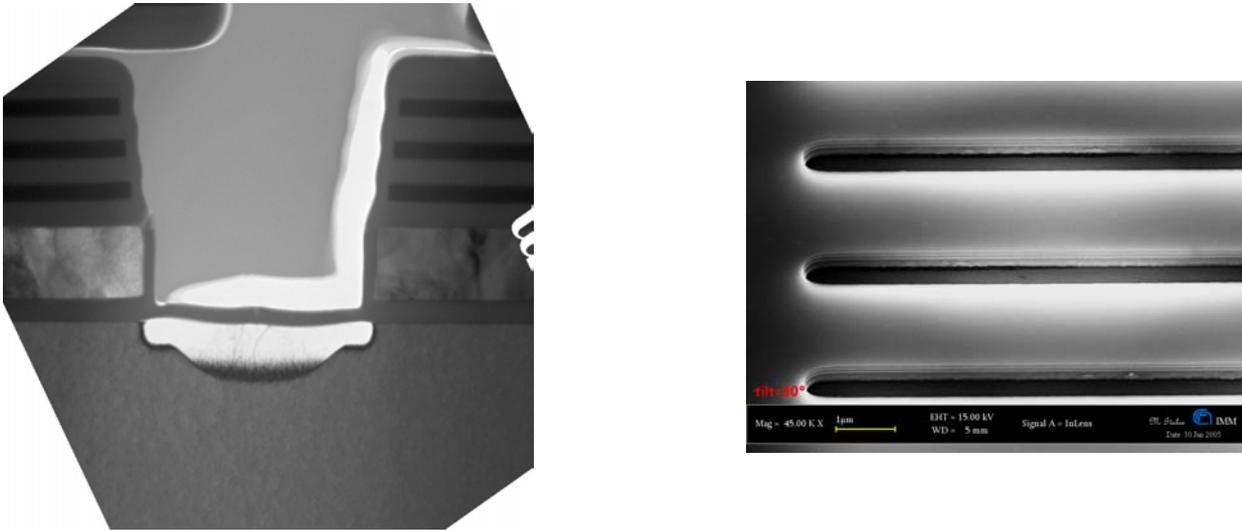


Fig. 13 TEM and SEM images of irradiated source regions in the test structure with dielectric mirrors.

In Fig. 13, the TEM image of the structure with the dielectric mirror patterned on top of the gate stack, after ELA, is shown; the poly-gate was well confined and no outflows were present.

The CLASS simulations of the gate stack including dielectric mirrors have confirmed the robustness of the new structure, indicating a threshold energy density for the beginning of melting of the poly-gate at 1.05 J/cm^2 .

Based on these promising results, it was decided to fabricate MOSFET's, adopting the new structure for the gate stack and including a 6 layer dielectric mirror.

The electrical results show a great improvement in terms of gate/source isolation with respect to the former structure. In the next table the yield and scraps values for ELA and standard RTP processes are compared.

	ELA process			Standard process
	850mJ/cm ²	900mJ/cm ²	950mJ/cm ²	
Oxide scraps	7.95 %	8.58 %	12.57 %	3.86 %
Junction scraps	0.38 %	0.63 %	0.6 %	0.96 %
Yield	91.7 %	90.8 %	86.8 %	95.2 %

Tab. 1 Yield comparison ELA and std process

Benefits to society

A scientific and technological contribution in the microelectronics field is certainly important for the development of Europe as an economic and cultural protagonist in a worldwide context. In fact, part of the economic power of the modern countries is based on their electronic know-how and telecommunication structures. The electronic device production implies the creation of a significant amount of job posts, with a consequent economic benefit for the European population, and improves the quality of life of the European citizens. The impact of electronics and telecommunications on human activities is in fact recognized in every field and at each level, from the health and safety to the education and information, or just to the simple welfare. Companies which use integrated circuits in their products can not survive without a strong and competitive semiconductor industry. In the objectives of the programme "Information Society Technologies" (IST), microelectronics is considered the foundation of the information society.

In order to benefit from the technological developments required for the future electronics, as reported by the IST work programme, Europe has to actively participate in the research work needed to achieve the results. The electronics companies are strongly dependent on the semiconductor industries and a solid European information society can only exist if high-tech semiconductor products are available. An alternative could be to rely on the high-tech devices produced in USA or Japan, but, apart from the lack of independence and vulnerability of Europe that this would generate, delegating this task to third parties would imply less highly specialised job posts in Europe, with a consequent loss of highly trained European specialists (physicists, chemists, electrical engineers, etc) to other continents.

The best route to explore the 65 nm CMOS technology is tracked by the European framework. Industries cannot afford the expenses, in terms of human resources, required to achieve the results needed to make the future technology feasible. The industrial environment is in fact mainly devoted to maintain the production rhythm and only limited efforts can be dedicated to experiments out-of-the-schemes. On the other hand, the public research institutions, though having the possibility to perform experiments under extreme conditions and being able to train and recruit young fellows who can carry out research on non conventional procedures, can hardly afford the huge costs and investments associated with these studies.

Within this context, the FLASH project played a leading-edge role to achieve processes and equipment for the 65 nm CMOS technology, joining expertise from both industry and public research institutions. The network formed to run the project activity was designed to assure European exploitation paths within the semiconductor industry. Both an equipment supplier, i.e.

Lambda Physik, as well as the third semiconductor industry in the world, i.e. STMicroelectronics, were involved to ensure the commercialisation of the results of the project.

As the FLASH workplan is based on the IST specifications, this shows both the European dimension and the industrial relevance.

In the objectives of the IST program, microelectronics as a key enabling technology was considered the foundation of the information society. Driving its development, enhancing its applicability, and accelerating its take-up in Europe, were some of the main goals of the program. In the work programme, the focus of this action line was on:

- (i) *New solutions for basic CMOS process modules (Si and Si/SiGe on bulk Si or SOI), on equipment related to the sub-topics below, and on integration of new materials. Simulation of processes, devices and equipment is included. Particular focus is on:
Front-end CMOS for technology nodes equal or below 70 nm.*
- (ii) *Innovative solutions for the major device, process and material integration challenges anticipated for the microelectronics technologies planned for industrialisation in the next 8-12 years. Focus is on:
Approaches based on alternative devices or architectures. The target performance and integration levels should be competitive with the 50 nm node of the ITRS roadmap and be viable beyond that point.*

With respect to the above specifications, the laser annealing method for the production of ultra-shallow junctions, can be considered as a viable strategy for keeping a competitive European know-how in the CMOS technology. No known solutions are available for the realisation of the ultra-shallow doped layers needed for the 65 nm node. The laser annealing method offers such a possibility, that could not be achieved by the conventional thermal processing currently used. Furthermore, the suggested work was in line also with the priority specifications related to the integration challenges planned for industrialization in the next 8-12 years. This long term research required to explore new frontiers in the field of dopant activation, such as laser based methods. The industrial relevance of the work is proven by several attempts of the ion implanters manufacturers, both in Europe and in the USA, to test the capabilities of the laser annealing method to achieve high performance ultra-shallow junctions.

Moreover, the continuous reduction of the feature size in ULSI MOS implies that various alternatives have to be tested and validated during process development and device design. This would require very high financial costs. Therefore, technology-computer-aided-design (TCAD)

tools, capable of simulating the interaction of the laser beam with the device structure, is crucial for pre-selection of technological options. The models developed within the project will fill the current gap that prevents accurate implementation of laser annealing in CMOS technology modelling.

Hence, the project activity included also the realization of a simulation software, capable of reproducing the physical phenomena that occur when a device structure is irradiated by a laser beam, that will offer new TCAD tools to the device manufacturers. These tools will then help to substantially reduce costs and time for design and optimization of devices. This aspect is as important as the production of reliable processing procedures.

The main applications of the present technology, developed within the frame of the FLASH project, are in the automotive and computing fields. With respect to the first area, the world-wide production of cars is expected to grow to about 70 million units in 2010, compared to the 56 million units produced in 2000. European car manufacturers must continue to be the drivers of innovation in vehicle technology as an important prerequisite for leadership in a market that is of extreme importance for the European economy and employment. Germany still produces around 25% of world production and about 1/7 of the country's jobs depend on the automotive industry. The European Semiconductor Industry plays a leading role in the development and production of components for the European Automotive market.

Nanoelectronics will provide the necessary sensors, computing power and reliability at affordable cost levels. To make these systems unobtrusive enough so that we do not end up resenting them, they must be small and easy to use. **They therefore put high demands on miniaturisation.**

A further important aspect was the development of skills in Europe. The three research institutes in the project employed a considerable amount of young fellows to perform the activities inherent to the project. They joined the institutions for their university degree or for the Ph.D. thesis, gained additional technical and management qualifications during their work under the supervision of senior scientists, and are now ready to join companies where they could have a highly specialized role. Thanks to the funding given for a project financed by the European Commission, this training and immediate employment could take place, giving rise to a clear social and economic impact.

Going beyond the state of the art technology is necessary to maintain and improve employment in the integrated circuits scenario. The extensive theoretical and experimental work proposed on the use of laser for the fabrication of the future CMOS devices towards the 65 nm technology node had a decisive role in the technological development leading to properly operating electronic nanodevices. Economic benefits will emerge from the possibility to find a new application of the laser sources in the semiconductor industry, both in terms of increased production of new tools by the equipment suppliers and competitiveness of the semiconductor industry. This

economic push is closely related to the social aspects relative to the employment in Europe, that would be beneficially influenced by the production of new tools and devices.

The reduction in the device size down to 65 nm will have an impact on all the application fields related to fundamental and complementary aspects of our daily life. They concern all the applications where the nano-sized and high speed electronic devices are a prime factor to be considered. Indeed, the FLASH project gave a contribution to this improvement of life of the European citizens.

Deliverables and references

The complete list of deliverables is reported here, along with a short description of the most relevant ones.

- D101 Dissemination and Use Plan (1 Apr 2003)
- D102 First progress report (18 Dec 2003)
- D103 Update of the project programme (8 Jul 2004)
- D104 Second Progress Report (23 Dec 2004)
- D105 Public Workshop for end users (20 Jan 2005)
- D106 Third Periodic Progress Report (1 Dec 2005)
- D107 Technology Implementation Plan (1 Mar 2006)

- D201 Specification on the irradiation of test structures under different laser annealing conditions (4 Dec 2003)
- D202 Specification on the integration of ELA in MOS process (14 Dec 2004)
- D203 Specification on ELA of wafers for MOS fabrication (26 Sept 2005)

- D301 Specification on the influence of ELA parameters on the redistribution and activation of As and B, including structural analysis of the samples (Included in the First Annual report)
- D302 Specification on the effect of atomic and molecular boron ions on electrical activation and chemical profile redistribution during ELA (7 Jun 2004)
- D303 Specification on the effect of the implant mask on the lateral diffusion following ELA (26 Nov 2004)
- D304 Specification on experimental data for TED during ELA-RTA processing (6 Sept 2005)
- D305 Specification on the optimized redistribution and activation of B and As following ELA-RTA (28 Nov 2005)

- D401 Release of the simulation tools based on continuum model for the thermal field and dopant evolution described by technical report (15 Dec 2003)
- D402 Specification on re-growing and segregation mechanism (13 Dec 2004)
- D403 Release of the updated version of the code, including the e.m. field simulation, described by technical report (2 Dec 2004)

D404 Specification on theoretical investigation of the defect generation at solid-liquid interface due to a laser annealing process (28 Jul 2005)

D405 Release of the updated versions of the codes, including also the modified packages for thermal process simulation described by technical report (28 Nov 2005)

D501 Specification on the electrical performance of test pattern (19 Jul 2004)

D502 Specification on the MOSFET fabrication flow chart (9 Dec 2004)

D503 Specification on the electrical measurements of MOSFET prototypes wafers (13 Jul 2005)

D504 Specification on the electrical performances of the packaged device (28 Nov 2005)

D105 – Public Workshop for end users

A workshop for end users will be held in Roma, on January 21st, 2005. The possibility to apply laser based methods, in order to anneal the implant damage and activate the dopant, is currently attracting both academic and industrial interest, because of its potential to overcome some technologic blocks and enable new technologies, as well as to allow a possible development of a new market segment, with possible economic consequences. The Workshop in Roma aimed to advertise the FLASH results to an audience of academic and industrial representatives, as well as it intended to open a forum where other groups and consortia, funded by national or international institutions, can express their ideas, solutions and skills. In order to do that, distinguished representatives have been invited to present the recent results on the application of non conventional thermal processing to semiconductor devices.

D203 – Specification on ELA of wafers for MOS fabrication.

Laser processing for Power MOSFET devices fabrication has been performed following the results on the integration of excimer laser annealing (ELA) in a MOSFET process, reported in Deliverable 202. The irradiations were performed at Lambda Physik, using the projection optics system, on patterned wafers processed at ST-Microelectronics. Three different runs have been performed using for the first and second run the optimised test structure described in D202, while in the third run a novel structure proposed by IFN-CNR, where the gate stack is shadowed by a dielectric mirror, was adopted. This last structure was also preliminary designed and tested.

D304 – Specification on experimental data for TED during ELA-RTA processing.

The TED (transient enhanced diffusion) of boron was studied using p-type Si(100) samples implanted with 10 keV boron ions (7° tilt, 30° twist angles) to a dose of $1 \times 10^{15} \text{ cm}^{-2}$. The ELA treatment was done using 10 pulses with an energy density of 1 J/cm^2 per pulse in vacuum with the samples at room temperature during the

irradiation. The RTA treatment has been carried out in N₂ ambient with a temperature ramp rate of ~200 °C/s. Chemical boron concentration and electrical activation profiles were measured by secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP), respectively.

No diffusion occurs in the tail region after ELA only, as reported in D302, and compared to that in samples without pre-treatment by ELA, a strongly suppressed TED of boron is found after subsequent RTA for 15-30 s at temperatures between 800 and 1100 °C. For instance, after RTA for 30 s at 800 °C, the diffusion length in the tail is reduced by a factor ~4 by pre-ELA (~5-7 versus ~20-30 nm). The pre-ELA is also beneficial for the electrical activation; subsequent RTA leads to almost complete activation (with only a minor inactive fraction) already at 800 °C while in samples subjected to RTA only temperatures of ~1100 °C are required for complete activation. The reduction in TED can be due to the liquid-state annealing of a fraction of the implantation induced excess self-interstitials. Secondly, besides the annealing, ELA is reported to introduce excess vacancies in the re-crystallized region. These vacancies can decrease the concentration of self-interstitials mediating the boron diffusion. Finally, solid state annealing of the defects by the heat wave propagating into the Si wafer can occur, as already illustrated by the observation of the electrical activation of boron in the region beyond the maximum melting depth (D302).

Using a very high boron concentration (>1 at %), obtained by implantation of 1 keV boron ions to a dose of 1×10^{16} cm⁻², both the as-implanted and ELA-pretreated samples exhibit so-called boron-enhanced diffusion (BED). A detailed study has revealed a time dependence of the BED, i.e. the enhancement decreases with time. However, ELA is not found to have any suppressing effect on the process(es) controlling BED.

D403 – Release of the updated versions of the codes, including also the electromagnetic simulation, described by a technical report

The deliverable consists in the release of the update version of the prototype tools for the simulation of the laser annealing process. The upgrade improves the accuracy of the two dimensional simulation of the thermal field evolution and the consequent dopant redistribution in Si-based structures as result of the laser irradiation. Indeed, while in the previous version of the code we have assumed the validity of the geometric optics rules for the estimate of the heat sources due to the irradiation, in the new version such sources are numerically estimated simulating the interaction between the laser pulse the transistor structure. We have implemented a Finite Difference Time Domain scheme for the simulation of the electromagnetic (e.m.) field. In the e.m simulation we use the same simulation box as in the case of thermal simulation. Therefore, the simulation box can be separated in different material zones distinguished by the proper thermal and optical parameters. A self consistent evaluation of the heat source is performed due to the occurrence of a liquid-solid phase transition which cause a change in the optical properties of the sample.

The codes features are described in a technical report. The report contains: a) a brief description of the FDTD method, b) details on the technique followed in the numerical implementation, c) the description of the codes capabilities, d) the discussion of test simulation results, e) comparisons between the results obtained with

the new and the old version of the code g) the comparison between the theoretical prediction and the experimental analysis of irradiated samples fabricated in the framework of the FLASH project.

D405 – Release of the updated versions of the codes, including also the modified packages for the thermal process simulation described by technical report.

We have implemented a code for the simulation the dopant diffusion during a Rapid Thermal Annealing process. This code simulates the non-equilibrium dopant diffusion in silicon in extrinsic condition and is based on the five-streams models. With the term “non-equilibrium diffusion” we indicate that the dopant diffusion occurs in presence of a defect (Interstitial (I) and Vacancy (V)) density exceeding the equilibrium one (super-saturation). With the term “extrinsic condition” we indicate that the dopant diffusion occurs in presence of a charge density exceeding the intrinsic silicon charge density at the RTA temperature considered. We have coupled the phase field model with a five-streams model for the dopant diffusion. The five-streams model assumes the validity of the kick-out mechanism for the dopants diffusion: i.e. the diffusion is triggered by the formation of defect-dopant mobile complex. The five streams are five coupled partial differential equation which formalize the model and rule the evolution of the dopants, vacancies, interstitials, vacancy-dopant pairs and interstitial-dopant pair. In the report we discuss: the model formalism, its calibration, the coupling with the laser annealing simulation, and the model predictions compared with experimental data obtained by the FLASH consortium.

D504 – Specification on the electrical performances of the packaged device

MOS devices with source layer activated by ELA have been packaged and characterized. On characteristics have been compared with standard devices with good results.

In this report:

- 1) the “on” characteristics of the first packaged MOS prototypes, according to project activity plan, have been analyzed;
- 2) the electrical characteristics of a second series of MOSFETs have been measured at wafer level. These prototypes, by exploiting the lateral diffusion less ELA process, have been realized with a shorter channel length, in order to obtain a gain in “on” resistance;
- 3) A third series of prototypes has been produced and electrically characterized at wafer level. These prototypes have been realized with a new structure, based on the use of a dielectric mirror gate stack, in order to reduce the ELA impact on the polycrystalline silicone gate electrode.

The FLASH consortium participated to several conferences, presenting the project. In particular, active participation of the partners occurred at:

- the Symposium “Advanced short time thermal processing for Si based CMOS devices” of the Electrochemical Society Spring Meeting in Paris, April 2003, with an oral presentation (“EXCIMER LASER ANNEALING: A SOLUTION FOR THE FUTURE TECHNOLOGY NODES?”) given by the coordinator.
- the Symposium “Materials science issues in advanced CMOS source-drain engineering”, of the European Materials Research Society (E-MRS), held in Strasbourg in May 2004, where two presentations were given by the partners and one invited presentation by the coordinator (“THE EUROPEAN ANSWER TO THE INTEGRATION ISSUES OF EXCIMER LASER ANNEALING IN MOS TECHNOLOGY” – “BORON-ENHANCED DIFFUSION IN EXCIMER LASER ANNEALED Si” – “COMPUTATIONAL METHODS FOR THE SIMULATION OF THE EXCIMER LASER ANNEALING IN MOS TECHNOLOGY”)
- to the 3rd International Conference “Computational Modeling and Simulation of Materials”, held in Acireale (Italy) in June 2004, with two presentations (“SIMULATION TOOLS FOR THE LASER PROCESS IN Si DEVICES” – “COMPUTATIONAL MODELLING AND SIMULATION OF MATERIALS”);
- to the Symposium C “Silicon front-end junction formation – physics and technology” of the Materials Research Society (MRS) Spring Meeting, held in San Francisco in April 2004, with one presentation (“TECHNOLOGY COMPUTER AIDED DESIGN OF ULTRA SHALLOW JUNCTIONS IN Si FORMED BY LASER ANNEALING”).
- the Symposium “Materials Science and Device issues for Future Si-based Technologies” of the European Materials Research Society (E-MRS), held in Strasbourg in May 2005, with two presentations (“BORON DISTRIBUTION IN SILICON AFTER EXCIMER LASER ANNEALING WITH MULTIPLE PULSES” – “EXCIMER LASER ANNEALING OF B AND BF₂ IMPLANTED Si”)
- the International Conference on Materials for Advanced Technologies 2005 (ICMAT 2005), organized by the International Union of the Materials Research Societies (IUMRS), held in Singapore in July 2005, with an invited

presentation by G. Fortunato (“EXCIMER LASER ANNEALING FOR SHALLOW JUNCTION FORMATION IN Si POWER MOS DEVICES”). The relative article, published on the journal “Thin solid films”, summarizes some of the main project results and groups all the participants to the project as co-authors.

- the 13th International Conference on Advanced Thermal Processing of Semiconductors (RTP), held in Santa Barbara (USA), October 2005, IEEE Conferences Series, Section “Laser annealing: technology, manufacturing and science”, with an Invited Lecture by A. La Magna (“MODELING AND SIMULATION OF LASER INTERACTION WITH SEMICONDUCTORS”)
- the Italian-Norwegian Bi-lateral Meeting organized by the Italian Embassy in Norway, held in Oslo, October 2005, with two presentations (“MODELS AND SIMULATION OF LASER ANNEALING” – “EXPERIMENTS OF LASER ANNEALING”)

Furthermore, several publications appeared in scientific journals, with high impact factors. The heading of some articles published in Applied Physics Letters (impact factor in 2004 4.308) are shown; they elucidate many fundamental aspects of the interaction between excimer laser beam and doped Si, both from the theoretical and experimental point of view.

Material modifications induced by laser annealing in two-dimensional structures

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During the first project year, a non disclosure agreement was signed by all the partners with ISE AG. ISE representatives were invited, and indeed they attended, to the FLASH partners meetings. The aim of such agreement was to evaluate the possibility of implementing the simulation programs, developed by the consortium within the frame of the project activity, into ISE commercial software packages for semiconductor industry.

Electrical activation phenomena induced by excimer laser annealing in B-implanted silicon

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APPLIED PHYSICS LETTERS **86**, 051909 (2005)

Depth distribution of B implanted in Si after excimer laser irradiation

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(Received 30 August 2004; accepted 30 November 2004; published online 28 January 2005)

APPLIED PHYSICS LETTERS **86**, 161905 (2005)

Role of light scattering in excimer laser annealing of Si

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(Received 6 December 2004; accepted 8 March 2005; published online 13 April 2005)

A phase-field approach to the simulation of the excimer laser annealing process in Si

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(Received 20 October 2003; accepted 9 February 2004)

Enhanced boron diffusion in excimer laser preannealed Si

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(Received 8 December 2004; accepted 24 February 2005; published online 4 April 2005)

Boron distribution in silicon after multiple pulse excimer laser annealing

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(Received 25 March 2005; accepted 5 July 2005; published online 15 August 2005)

The effect of excimer laser pretreatment on diffusion and activation of boron implanted in silicon

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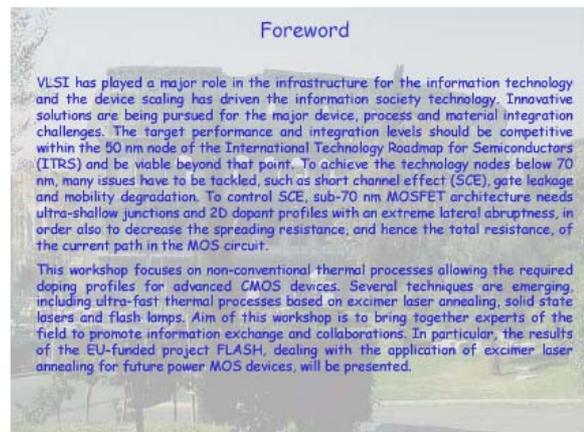
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(Received 24 June 2005; accepted 12 September 2005)

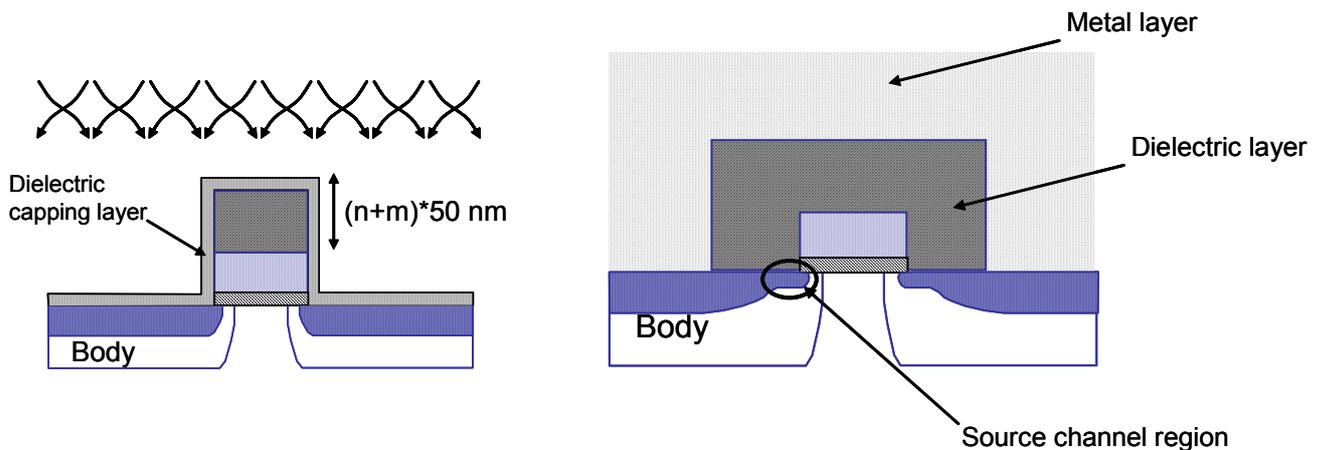
As planned among the dissemination activities of the project, a workshop for end users was held in Roma on January 21st, 2005. The possibility to apply laser based methods, to anneal the implant damage and activate the dopant, is currently attracting the interest of several suppliers of the semiconductor industry, as well as of this industry itself. The former are concerned of a possible development of a new market segment, with possible economic consequences, while the latter are interested to a potential solution for overcoming some technologic blocks and enabling new technologies, also in this case accompanied by an economic impact.



The Workshop in Roma advertised the FLASH results to an audience of academic and industrial representatives, as well as provided a forum where other groups and consortia, funded by national or international institutions, expressed their ideas, solutions and skills. In order to do that, distinguished representatives were invited to present the recent results on the application of non conventional thermal processing to semiconductor devices,

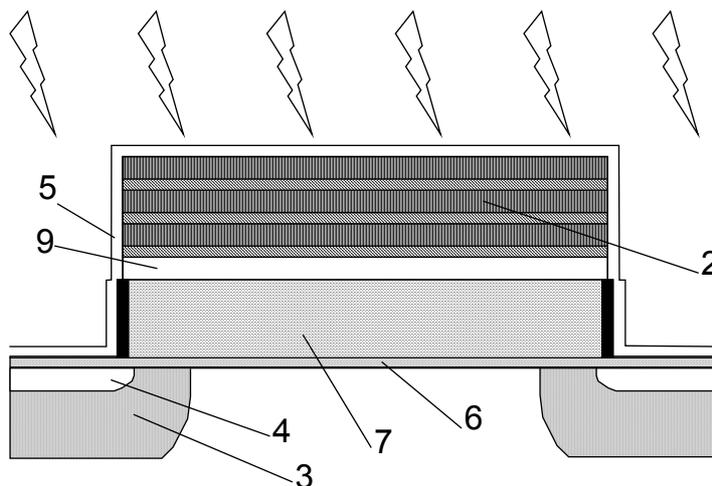
The protection of the intellectual property was also considered within the frame of the project. Two patent proposals were hence filed at the European Patent Office: “High scale integration MOS device” (F. Simon, A. Magri, G. Fortunato, V. Privitera) and, with the same title, “High scale integration MOS device” (D. Salinas, A. Magri, M. Camalleri, G. Fortunato, L. Mariucci, M. Cuscunà). The submission of the patent proposal has been managed by ST, but the affiliation of the authors is broadly distributed among the partner institutions.

The first patent is relative to Off Axis Irradiation. The proposal discusses a method to fabricate a high scale integration MOS device by using an off axis laser irradiation. The splitted laser beam is



obtained by a special optics system that provides two beams oriented with respects to device surface with a tilt angle.

The second patent instead concerns the approach used to shield the laser radiation, based on the dielectric mirror on top of the polycrystalline silicon gate. The proposal discusses the method to



fabricate a high scale integration MOS device by using the dielectric mirror to protect the gate structure. The dielectric mirror is realized by dielectric layers and plays an active function in the electric isolation of the MOS electrodes.

Finally, the first prize for the best presentation was awarded to the project coordinator (*Perspectives and advantages of the use of laser in the MOS technology*) at the Italian Physical Society Annual Conference, held in September 2005. This definitely represents a joint achievement of the FLASH partners.

<p>Scientific or technical publications on reviewed journals and conferences</p>	<p>A. La Magna, P. Alippi, V. Privitera, G. Fortunato, M. Camalleri, B. Svensson, "A phase field approach to the simulation of the excimer laser annealing process in Si", J. Appl. Phys. 95, 4806 (2004). CNR-IMM, CNR-IFN, STMicroelectronics, University of Oslo</p> <p>A. La Magna, P. Alippi, V. Privitera, S. Scalese, S. Pannitteri, G. Fortunato, L. Mariucci, M. Camalleri, "Material modifications induced by laser annealing in two-dimensional structures", Appl. Phys. Lett. 84, 4738 (2004). CNR-IMM, CNR-IFN, STMicroelectronics</p> <p>"Phase-field simulations of the laser annealing process in Si-devices", A. La Magna, P. Alippi, V. Privitera, G. Fortunato, M. Camalleri and B. Svensson 3rd International Conference "Computational Modeling and Simulation of Materials", Acireale (Italy) 2004. CNR-IMM, CNR-IFN, STMicroelectronics, University of Oslo</p> <p>"Simulation tools for the laser process in Si device manufacturing", A. La Magna, P. Alippi, V. Privitera, G. Fortunato 3rd International Conference "Computational Modeling and Simulation of Materials", Acireale (Italy) 2004. CNR-IMM, CNR-IFN</p> <p>"Technology computer aided design of ultra-shallow junctions in Si devices formed by laser annealing processes", A. La Magna, P. Alippi, V. Privitera, G. Fortunato, M. Camalleri and B. Svensson Symposium C "Silicon front-end junction formation – physics and technology" Materials Research Society (MRS) Spring Meeting, San Francisco (USA), April 2004. CNR-IMM, CNR-IFN, STMicroelectronics, University of Oslo</p> <p>"Computational methods for the simulation of excimer laser annealing in MOS technology" A. La Magna, P. Alippi, V. Privitera, G. Fortunato, L. Mariucci and M. Camalleri Symposium B "Material science issues in advanced CMOS source-drain engineering" European Materials Research Society (E-MRS) Conference, Strasbourg May 2004. CNR-IMM, CNR-IFN, STMicroelectronics</p> <p>"Boron-enhanced diffusion in excimer laser annealed Si" E.V Monakov, B.G. Svensson, M.K. Linnarsson, A. LaMagna, V. Privitera, G. Fortunato and L. Mariucci; Materials Science & Engineering B (2004), in press and presented at E-MRS04</p>
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UniOslo, CNR-IMM, CNR-IFN

"Excimer laser annealing of shallow As and B doped layers"

E.V. Monakov, B.G. Svensson, M.K. Linnarsson, A. LaMagna, V. Privitera, M. Camalleri, G. Fortunato and L. Mariucci; **Materials Science & Engineering B (2004), in press and presented at EMRS04**

and presented at E-MRS04

UniOslo, CNR-IMM, CNR-IFN

"Electrical activation phenomena induced by excimer laser annealing in B-implanted silicon"

G. Fortunato, L. Mariucci, A. LaMagna, P. Alippi, M. Italia, V. Privitera, B.G. Svensson and E.V. Monakov, **Appl. Phys. Lett. 85, 2268 (2004)**

CNR-IFN, CNR-IMM, UniOslo

G. Mannino, V. Privitera, A. La Magna, E. Rimini, E. Napolitani, G. Fortunato, and L. Mariucci, "Depth distribution of B implanted in Si after excimer laser irradiation", **Appl. Phys. Lett. 86, 051909 (2005).**

A. La Magna, P. Alippi, V. Privitera, G. Fortunato, "Role of light scattering in excimer laser annealing of Si", **Appl. Phys. Lett. 86, 161905 (2005).**

The effect of excimer laser pre-treatment on diffusion and activation of boron implanted in silicon"

E.V. Monakhov, B.G. Svensson, M.K. Linnarsson, A. La Magna, M. Italia, V. Privitera, G. Fortunato, M. Cuscuno and L. Mariucci, **Appl. Phys. Lett. 87, 192109 (2005).**

"Boron Distribution in Silicon After Multiple Pulse Excimer Laser Annealing"

E. V. Monakhov, B. G. Svensson, M. K. Linnarsson, A. La Magna, M. Italia, V. Privitera, G. Fortunato, M. Cuscuno and L. Mariucci, **Appl. Phys. Lett. 87, 081901 (2005).**

"Excimer laser annealing of B and BF₂ implanted Si"

E.V. Monakhov, B.G. Svensson, M.K. Linnarsson, A. La Magna, M. Italia, V. Privitera, G. Fortunato, M. Cuscunà, and L. Mariucci, **Materials Science and Engineering B, (2005).**

"Boron distribution in silicon after excimer laser annealing with multiple pulses"

E.V. Monakhov, B.G. Svensson, M.K. Linnarsson, A. La Magna, M. Italia, V. Privitera, G. Fortunato, M. Cuscunà and L. Mariucci, **Materials Science and Engineering B, (2005).**

"Enhanced boron diffusion in excimer laser pre-annealed Si"

E.V. Monakhov, B.G. Svensson, M.K. Linnarsson, A. La Magna, C. Spinella, C. Bongiorno, V. Privitera, G. Fortunato and L. Mariucci, **Appl. Phys. Lett. 86, 151902 (2005).**

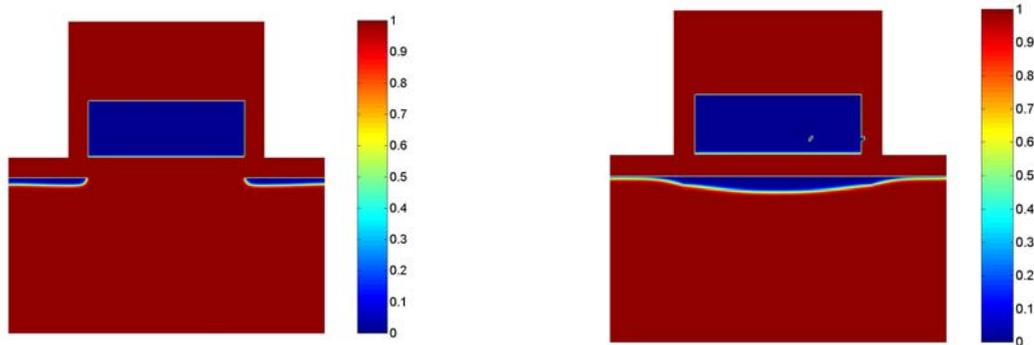
<p>Invited papers published in scientific or technical journal or conference.</p>	<p>Title and journals/conference and partners involved “The European answer to the integration issues of Excimer Laser Annealing in MOS technology” V. Privitera, A. La Magna, G. Fortunato, M. Camalleri, A. Magri, F. Simon, B.G. Svensson Symposium B “Material science issues in advanced CMOS source-drain engineering” European Materials Research Society (E-MRS) Conference, Strasbourg May 2004. CNR-IMM, CNR-IFN, STMicroelectronics, MicroLas/Lambda Physik, University of Oslo</p> <p>A. La Magna, “MODELING AND SIMULATION OF LASER INTERACTION WITH SEMICONDUCTORS”, Invited Lecture at the Section “Laser annealing: technology, manufacturing and science” of the 13th International Conference on Advanced Thermal Processing of Semiconductors (RTP), Santa Barbara (USA), October 2005, IEEE Conferences Series.</p> <p>G. Fortunato, “EXCIMER LASER ANNEALING FOR SHALLOW JUNCTION FORMATION IN Si POWER MOS DEVICES”, Invited Talk at the International Conference on Materials for Advanced Technologies 2005 (ICMAT 2005), Singapore, July 2005, organized by the International Union of the Materials Research Societies (IUMRS).</p>
<p>Patents filed and pending</p>	<p>November 15th, 2005 – EUROPEAN UNION</p> <p>High scale integration MOS device D. Salinas, A. Magri, M. Camalleri (ST) G. Fortunato, L. Mariucci, M. Cuscunà (CNR) Method to fabricate a high scale integration MOS device by using a dielectric mirror to protect the gate structure from laser annealing. The dielectric mirror is realized by dielectric layers and it has an active function in MOS electrodes electric isolation..</p> <p>High scale integration MOS device F. Simon (Lambda Physik), A. Magri (ST), G. Fortunato (CNR), V. Privitera (CNR) Method to fabricate a high scale integration MOS device by using an off axis laser irradiation. The splitted laser beam is obtained by a special optics system that provides two beams oriented with respects to device surface with a tilt angle.</p>
<p>Media appearances and general publications (articles, press releases, etc.)</p>	<p>References: IST Results http://istresults.cordis.lu/index.cfm?section=news&tpl=article&BrowsingType=Features&id=74884 “Life beyond CMOS” Interview with the project coordinator V. Privitera</p> <p>Almanacco della Scienza</p>

	<p>Rivista on line del Consiglio Nazionale delle Ricerche, N.16 del 19/10/2005 http://150.146.47.106/rivistaonline/base_lente.asp?IDrubrica=5&nomeFile=05_16_2005 "Transistor al laser: ora sono realtà" Interview with the project coordinator V. Privitera</p>
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FUTURE OUTLOOK

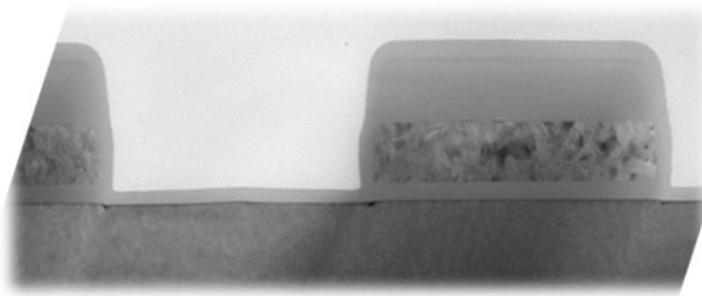
The vision at the end of the project is clear: the outcomes gained do not have to be considered only as achieved targets, but rather they have to be as a platform for transformation in the field of thermal processing of future CMOS technology nodes. This in turn implies that the solutions released by the consortium, relative to low power electronics, should be evaluated for their application to scaled CMOS technologies. The consortium is indeed quite confident on the possibility of success of the ELA process in the latter case, based on the experiments led during the project and their deep interpretation. However, without electrical testing of a prototype, no conclusive answer can be given on the reliability of the processing method, as we have clearly elucidated in the FLASH project. The documented heritage of the project is contained in the publications and the patents released by the consortium, that are consultable by the external academic and industrial groups eventually willing to extend this method to 65 nm CMOS and beyond. Nevertheless, close to the end of the project, the consortium initiated some experiments in order to evaluate the first order issues of applying ELA to scaled structures.

The impact of the ELA process onto scaled device geometries has been thus investigated, both theoretically and experimentally. The implanted window in this test structure is $0.25\ \mu\text{m}$, while the As implant was made with an energy of 10 keV, instead of 40 keV as in the transistor, that



generates an amorphous layer of about 20 nm. The gate stack was scaled as well, using a 100 nm thick polycrystalline silicon layer. The simulation results, obtained by CLASS, indicate that a much lower laser fluence has to be used for a proper annealing of the junction; this is due to the thinner gate electrode, that does not prevent the underlying channel region from melting, if energy densities above $500\ \text{mJ}/\text{cm}^2$ are used. Not negligible, however, are the optical effects that yield

more absorption in the polycrystalline silicon than in the increasingly narrower slit/window. The implanted structures were irradiated, based on the conditions suggested by the E.M. field / thermal simulations, i.e. at much lower energy. The implant damage is efficiently removed at such low energy, as it was indicated by the simulation, so providing a positive result from the structural point of view. Of course, other changes should be made to the structure for testing the feasibility of the process, as, for example, we have used a thick gate oxide, as that of the power transistor. Nevertheless, this result shows that sufficient radiation for annealing the source implant damage is



Scaled device structure, implanted with 10 keV As at high dose, after a 490 mJ/cm² irradiation. The implantation defects are efficiently removed in this scaled structure by low energy laser irradiation.

adsorbed through the narrow slit, whereas the gate electrode is not altered by the radiation and does not show any evident structural modification, as shown by the TEM below. This is just a quick and preliminary test, but certainly more reliable results might be obtained by applying other solutions presented by the consortium, such as the dielectric mirror gate, that would shield the gate stack from the incident radiation up to 90%. Even if no data are available and only hypotheses can be formulated at this stage, significant possibilities of success appear likely to occur.

The project results have shown that ELA can be successfully integrated in the MOS technology, providing high performances with high yield, while preliminary tests indicate that an extension to other device technologies might be possible, taking advantage of the project experimental and theoretical outcomes.