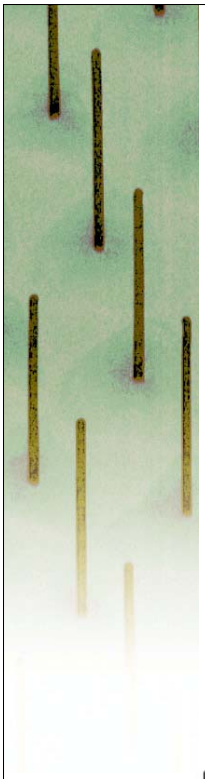
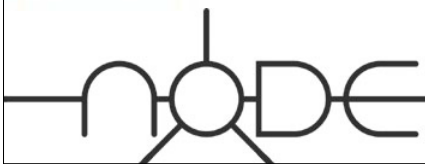
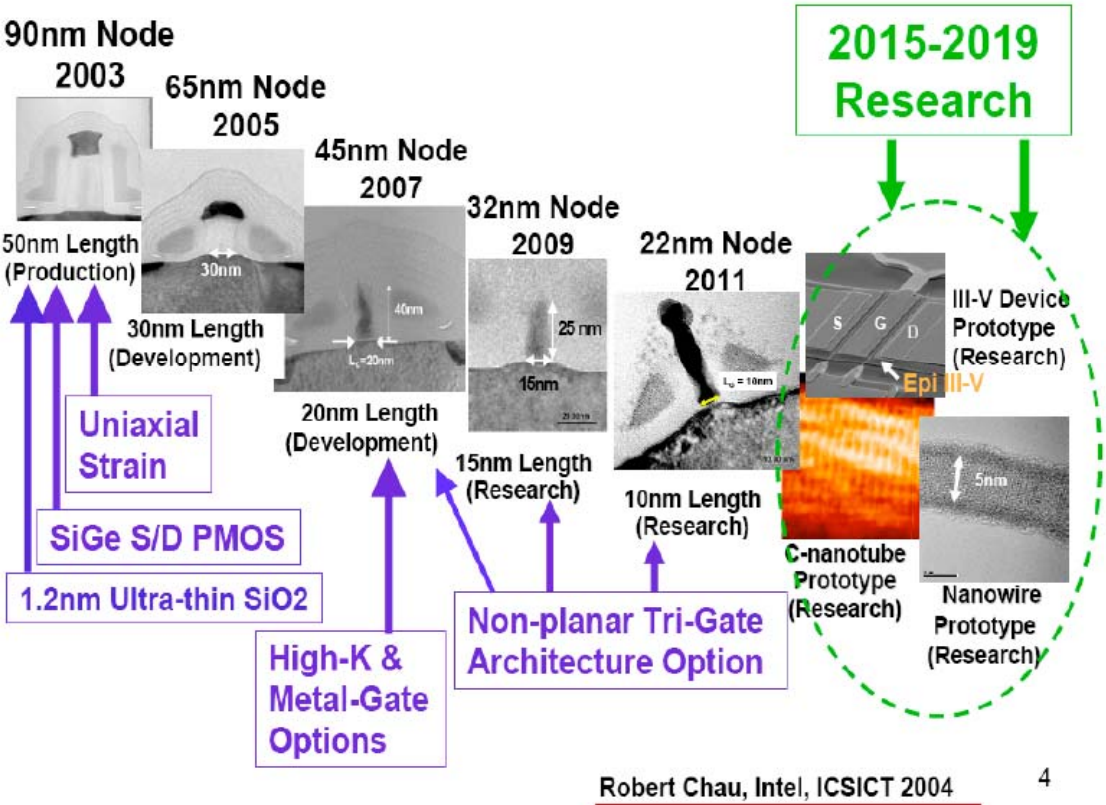


NODE

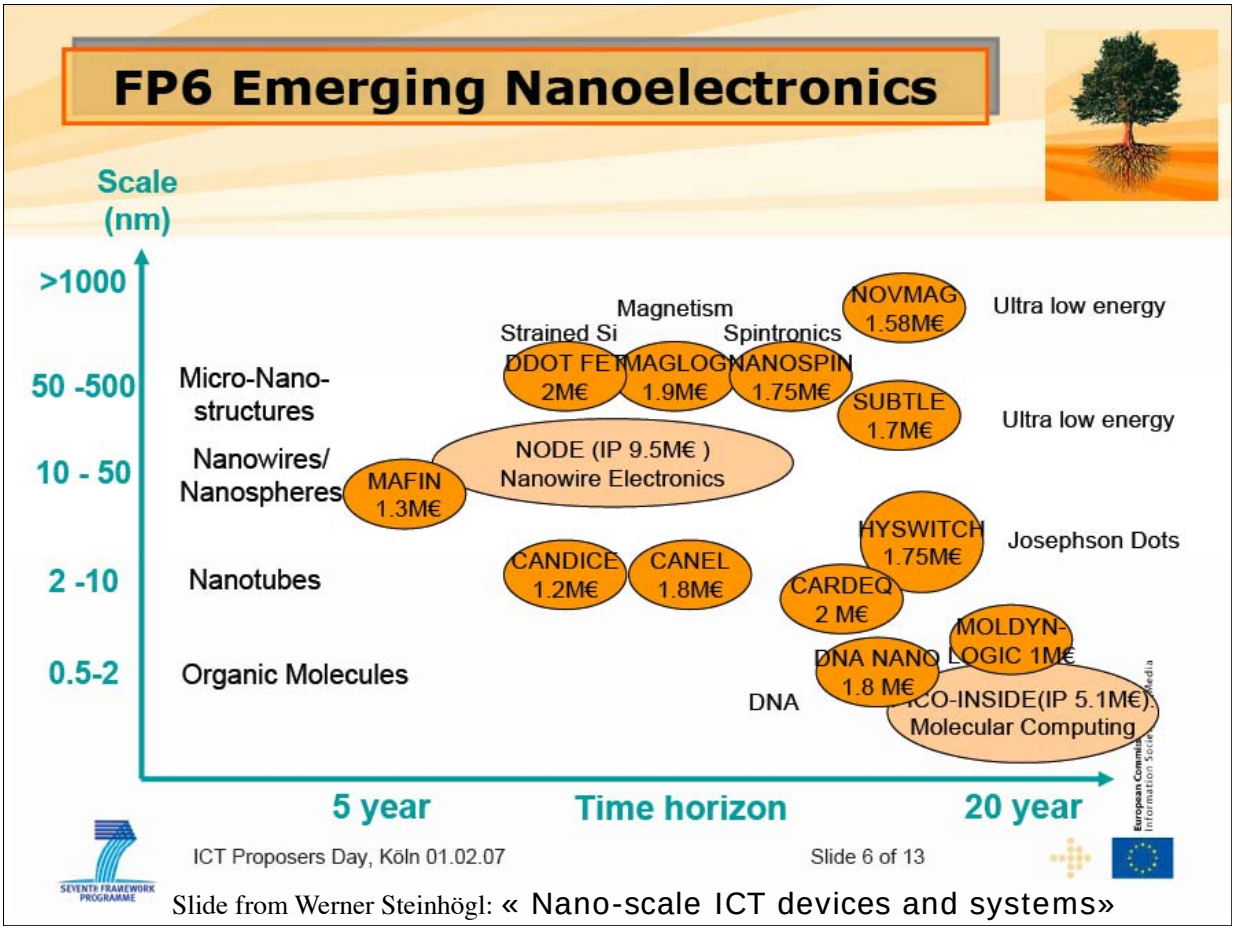
Nanowire-based One-Dimensional Electronics



Transistor Scaling and Research Roadmap



Robert Chau, Intel, ICSICT 2004



Slide from Werner Steinhögl: « Nano-scale ICT devices and systems»

"NODE"

NANOWIRE-BASED ONE-DIMENSIONAL ELECTRONICS

SIXTH FRAMEWORK PROGRAMME

An Integrated Project in EU FP6
Information Society Technologies (IST)

Project abstract

NODE focuses on an innovative bottom-up approach to fabrication and integration of nanoelectronic devices, based on self-assembling semiconductor nanowires. The primary target is to deliver replacement and add-on technologies to silicon CMOS, such as FET devices for logics and III-V bipolar transistors for RF applications. NODE will study key device families based on semiconductor nanowires, assess their compatibility with conventional semiconductor processing, and evaluate novel architectural concepts and their implementation scenarios.

Short facts about NODE

EC contribution:	€ 9 496 000
Number of partners:	12
Coordinator:	Lund University, Sweden
Start date:	September 1st 2005
Project length:	48 months
Universities:	4
Research institutes:	3
Companies:	5 (1 SME)

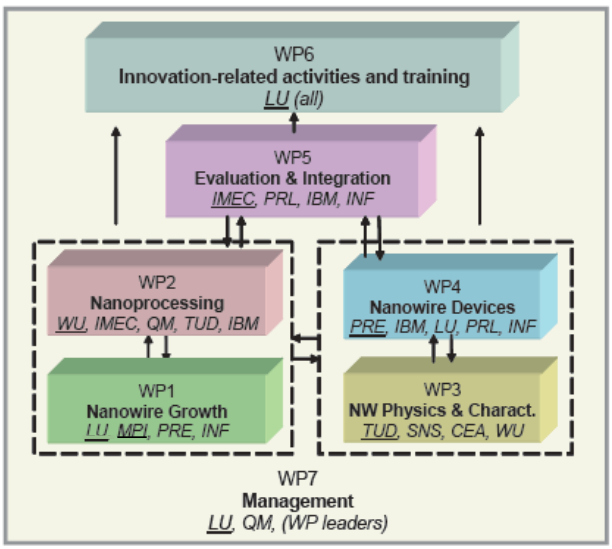
www.node-project.com

nanowire-based one-dimensional electronics

Specific competences among NODE partners:

Participants	
Lunds universitet	III-V NW growth, NW-Devices
Philips Electronics Nederland B.V.	III-V NW growth, NW-Devices
Technische Universiteit Delft	Electrical char., Processing
Max Planck Gesellschaft zur Foerderung der Wissenschaften	Si NW growth
Bayerische Julius – Maximilians Universität Würzburg	Processing, Optical char.
Scuola Normale Superiore	Heterostr. design, Optics
IBM Research GmbH	Si NW growth, Proc/Integr.
Interuniversitair Micro-Elektronica Centrum vzw	Processing, Si integration
Qumat Technologies AB	Processing
Qimonda Dresden GmbH & Co. OHG	Si NW memories, Si integr.
Commissariat á l'Energie Atomique	X-ray struct. char., Modelling
NXP Semiconductors Belgium NV	NW-Devices, Si integration

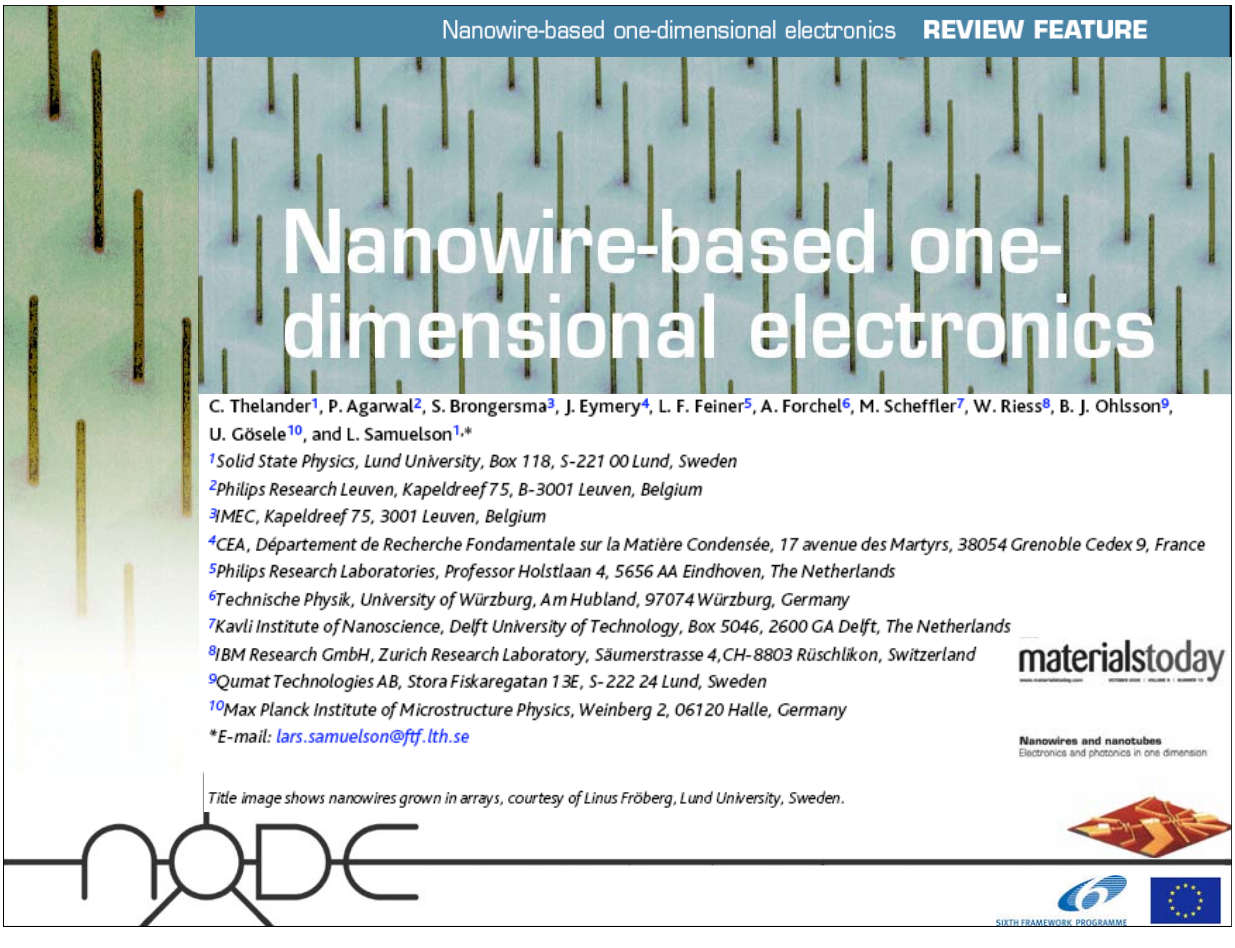
Work package structure



Research in NODE

Work packages	Main tasks and objectives	Partners
WP1 Nanowire Growth	**WP Leader: Peter Werner (MPI)** • Basic growth control • Doping control • Heterostructures (vertical and radial) • Epitaxial growth on silicon • Development of Si-compatible catalysts	LU INF MPI PRE
WP2 Nanoprocessing	**WP Leader: Alfred Forchel (WU)** • Vertical NW processing • Planarization and wire end Ohmic contacts • Gates to nanowires (Si, III/Vs) • Scalable catalyst positioning for NW growth	WU IBM IMEC QM TUD
WP3 Nanowire Physics & Characterization	**WP Leader: Leo Kouwenhoven (TUD)** • Control of surface states on nanowires • Investigation of 1D specific properties • Structural characterization of NWs • Transport in NW heterostructures, including superlattices	TUD CEA SNS WU
WP4 Nanowire Devices	**WP Leader: Louis-Félix Feiner (PRE)** • Build nanowire transistors (FET, bipolar) • Explore nanowire-based logic elements • Study nanowire-based memories • Explore nanowire light sources for on-chip communication	PRE IBM INF LU PRL
WP5 Evaluation & Integration	**WP Leader: Philippe Vereecken (IMEC)** • Benchmark nanowire devices • Explore SI-technology integration potential • Evaluate potential for NW circuits and architectures	IMEC IBM INF PRL
WP6 Innovation related activities and training	**WP Leader: Martin Magnusson (LU)** • Dissemination • Exploitation • IPR • Training activities	LU (all)
WP7 Management	**WP Leader: Lars Samuelson (LU)** • Organize meetings • Monitor project progress • Coordination of report writing	LU QM (WP leaders)

SIXTH FRAMEWORK PROGRAMME



Nanowire-based one-dimensional electronics

C. Thelander[1], P. Agarwal[2], S. Brongersma[3], J. Eymery[4], L. F. Feiner[5], A. Forchel[6], M. Scheffler[7], W. Riess[8], B. J. Ohlsson[9], U. Gösele[10], and L. Samuelson[1,*]

[1]Solid State Physics, Lund University, Box 118, S-221 00 Lund, Sweden
[2]Philips Research Leuven, Kapeldreef 75, B-3001 Leuven, Belgium
[3]IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[4]CEA, Département de Recherche Fondamentale sur la Matière Condensée, 17 avenue des Martyrs, 38054 Grenoble Cedex 9, France
[5]Philips Research Laboratories, Professor Holstlaan 4, 5656 AA Eindhoven, The Netherlands
[6]Technische Physik, University of Würzburg, Am Hubland, 97074 Würzburg, Germany
[7]Kavli Institute of Nanoscience, Delft University of Technology, Box 5046, 2600 GA Delft, The Netherlands
[8]IBM Research GmbH, Zurich Research Laboratory, Säumerstrasse 4,CH-8803 Rüschlikon, Switzerland
[9]Qumat Technologies AB, Stora Fiskaregatan 13E, S-222 24 Lund, Sweden
[10]Max Planck Institute of Microstructure Physics, Weinberg 2, 06120 Halle, Germany
*E-mail: lars.samuelson@ftf.lth.se

materialstoday

Nanowires and nanotubes
Electronics and photonics in one dimension

Title image shows nanowires grown in arrays, courtesy of Linus Fröberg, Lund University, Sweden.

SIXTH FRAMEWORK PROGRAMME

Work performed during the 2nd year:

WP1: NANOWIRE GROWTH

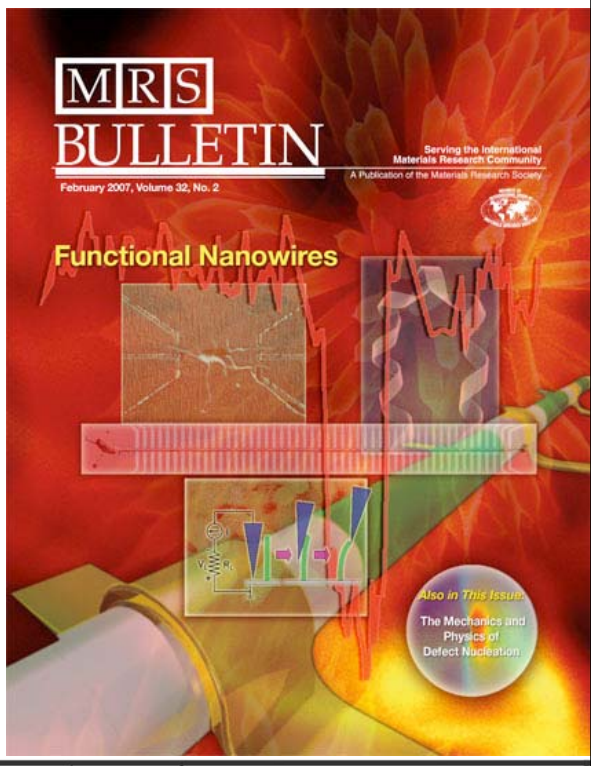
- Studies of catalytic and non-catalytic NW growth
- Evaluation of heterostructure formation and doping
- Growth of NWs on silicon substrates

Epitaxial Growth of III–V Nanowires on Group IV Substrates

Erik P.A.M. Bakkers, Magnus T. Borgström, and Marcel A. Verheijen

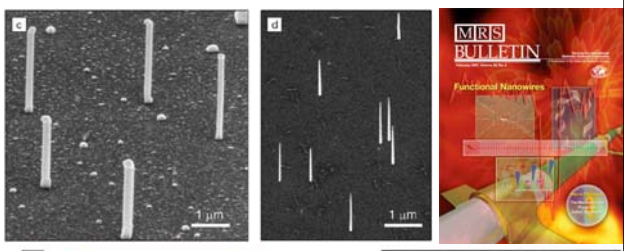
Directed Growth of Branched Nanowire Structures

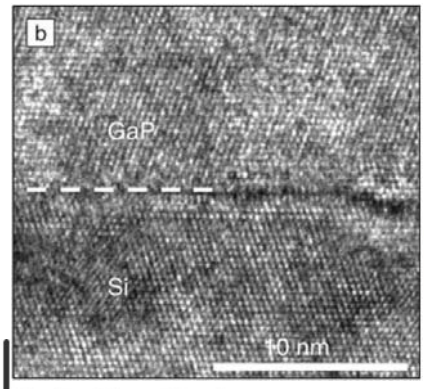
Kimberly A. Dick, Knut Deppert, Lisa S. Karlsson, Magnus W. Larsson, Werner Seifert, L. Reine Wallenberg, and Lars Samuelson

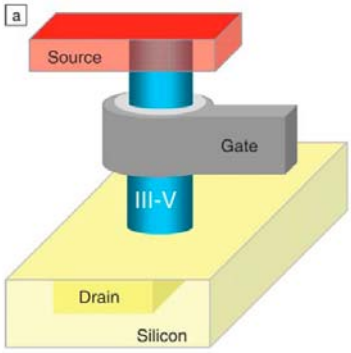


Epitaxial Growth of III–V Nanowires on Group IV Substrates

Erik P.A.M. Bakkers, Magnus T. Borgström, and Marcel A. Verheijen







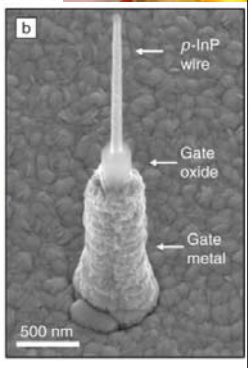
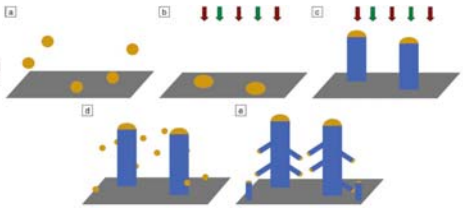
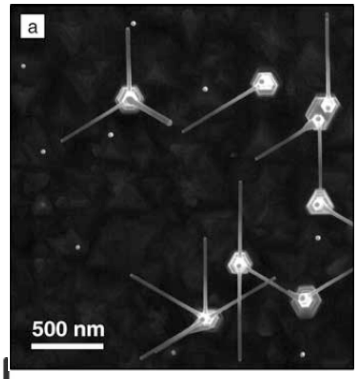


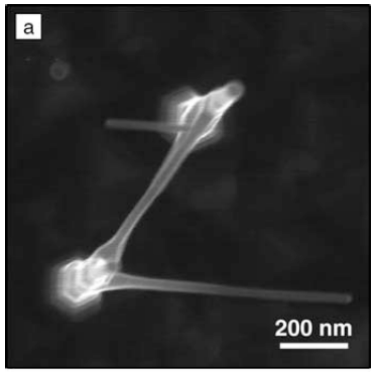
Figure 5. (a) Schematic illustration of a vertical nanowire transistor. The active channel is a III–V nanowire epitaxially connected to the silicon substrate, and the gate is wrapped around the channel. (b) Scanning electron micrograph (side view, 30°) of a nearly finished vertical device consisting of a p-type InP wire covered with gate oxide and gate metal.

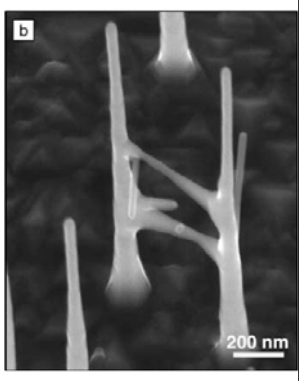
Directed Growth of Branched Nanowire Structures

Kimberly A. Dick, Knut Deppert, Lisa S. Karlsson, Magnus W. Larsson, Werner Seifert, L. Reine Wallenberg, and Lars Samuelson









See also: Dick et al. “Position-controlled interconnected InAs NW networks”, NanoLett 6 (12), 2842 (2006)

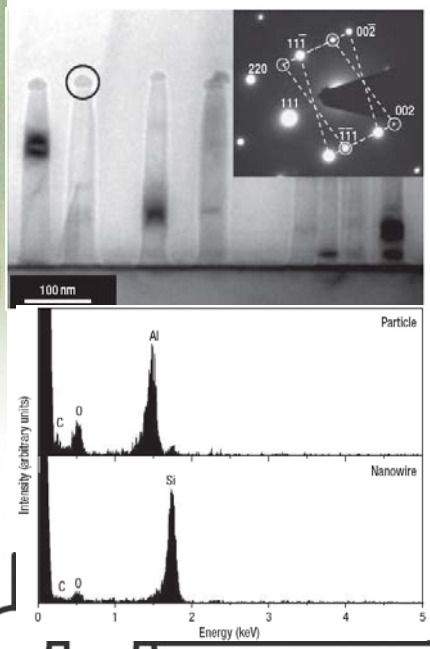
nature nanotechnology | VOL 1 | DECEMBER 2006 | 186

LETTERS

Epitaxial growth of silicon nanowires using an aluminium catalyst

YEWU WANG*†, VOLKER SCHMIDT*, STEPHAN SENZ AND ULRICH GÖSELE

Max Planck Institute of Microstructure Physics, Weinberg 2, 06120 Halle, Germany



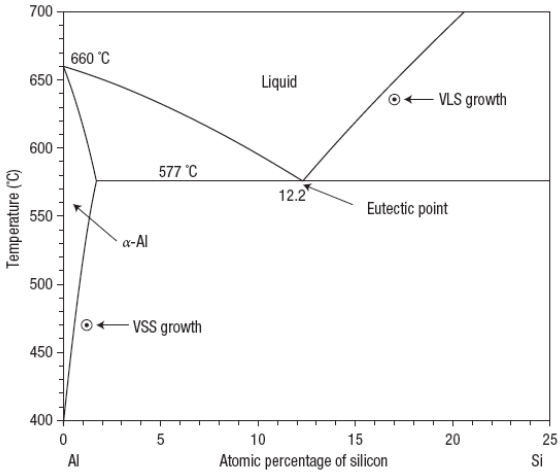


Figure 1 Schematic of the Al-rich region of the Al–Si binary phase diagram (data from ref. 16). VLS and VSS are indicated for arbitrarily chosen temperatures.

Advanced Materials Vol 19, No 14; 16 July 2007

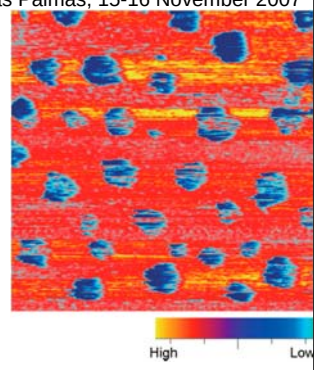
ADVANCED MATERIALS

COMMUNICATION

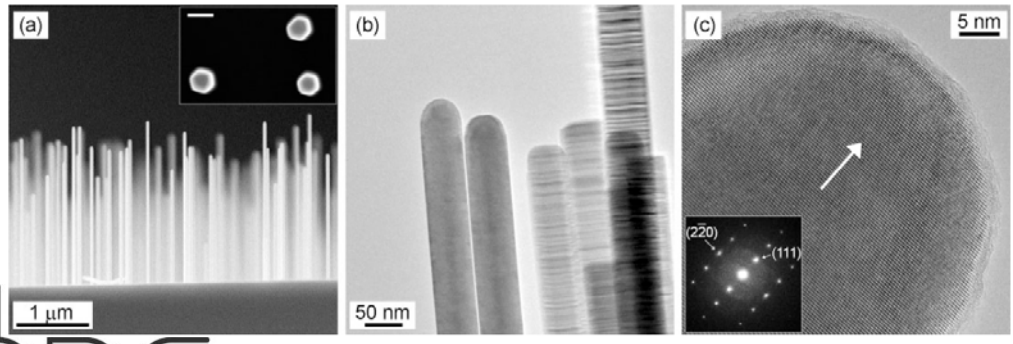
DOI: 10.1002/adma.200700285

Epitaxial Growth of Indium Arsenide Nanowires on Silicon Using Nucleation Templates Formed by Self-Assembled Organic Coatings**

By *Thomas Mårtensson, Jakob B. Wagner, Emelie Hilner, Anders Mikkelsen, Claes Thelander, Julian Stangl, Björn Jonas Ohlsson, Anders Gustafsson, Edvin Lundgren, Lars Samuelson,* and Werner Seifert*



- Large area patterning possible
- Avoids Au completely
- Excellent uniformity & growth control
- Next: methods for position control & FETs on Si



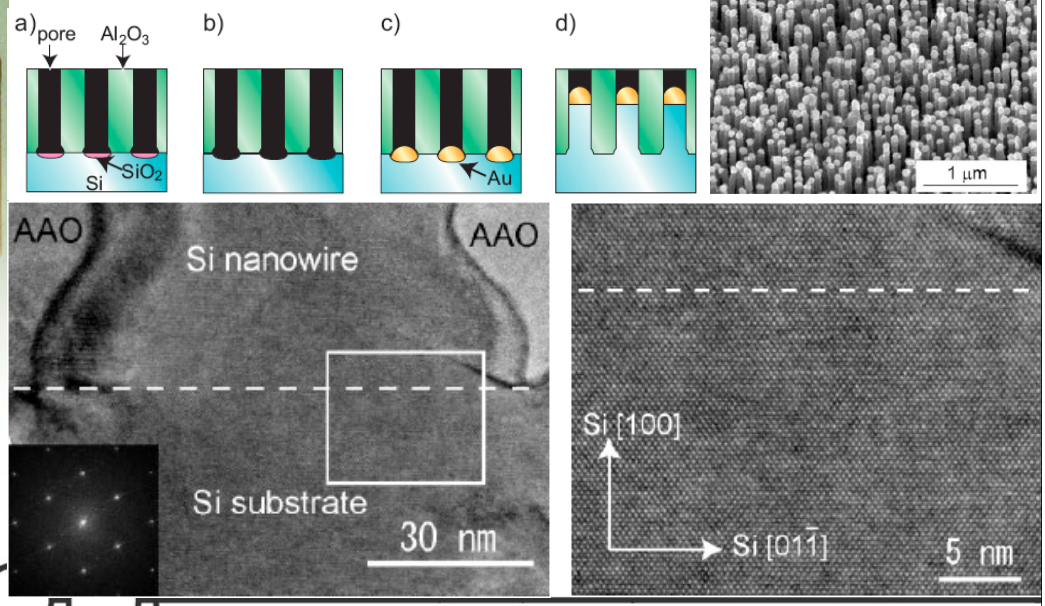
ADVANCED MATERIALS

DOI: 10.1002/adma.200700153

Adv. Mater. 2007, 19, 917–920

Synthesis of Vertical High-Density Epitaxial Si(100) Nanowire Arrays on a Si(100) Substrate Using an Anodic Aluminum Oxide Template**

By Tomohiro Shimizu,* Tian Xie, Jo Nishikawa, Shoso Shingubara, Stephan Senz, Ulrich Gösele



Work performed during the 2nd year:

WP1: NANOWIRE GROWTH

- Studies of catalytic and non-catalytic NW growth
- Evaluation of heterostructure formation and doping
- Growth of NWs on silicon substrates

WP2: NANOPROCESSING

- Studies of NW-dielectric interfaces
- Development of ALD of high-k dielectrics
- Implementation of wrap-gate technologies for FETs

APPLIED PHYSICS LETTERS **90**, 142110 (2007)

Vertical surround-gated silicon nanowire impact ionization field-effect transistors

M. T. Björk,[a] O. Hayden, H. Schmid, H. Riel, and W. Riess
IBM Research GmbH, Zurich Research Laboratory, Säumerstrasse 4, 8803 Rüschlikon, Switzerland

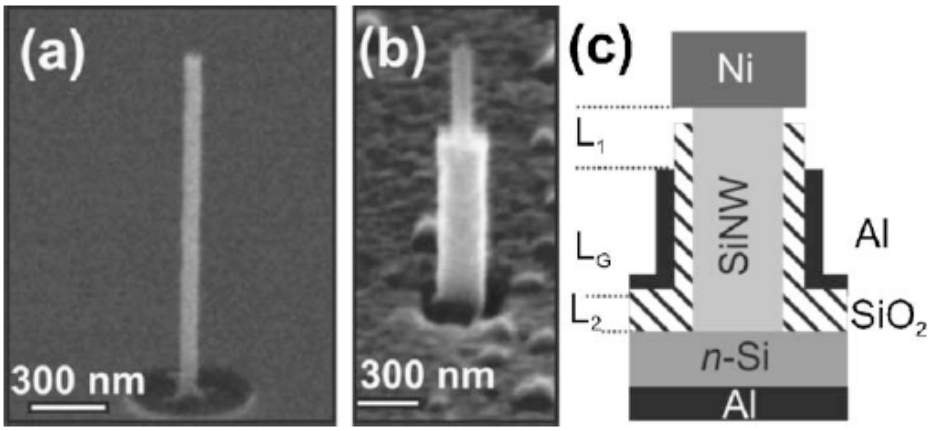


FIG. 1. Processing of vertical Si NW transistors. (a) 60-nm-diameter Si wire covered with 25 nm SiO_2 gate dielectric. (b) Wire with gate length defined by etching of Al. (c) Schematics of the surround-gated transistor displaying the gate length L_G and ungated regions L_1 and L_2.

Work performed during the 2nd year:

WP1: NANOWIRE GROWTH
- Studies of catalytic and non-catalytic NW growth
- Evaluation of heterostructure formation and doping
- Growth of NWs on silicon substrates

WP2: NANOPROCESSING
- Studies of NW-dielectric interfaces
- Development of ALD of high-k dielectrics
- Implementation of wrap-gate technologies for FETs

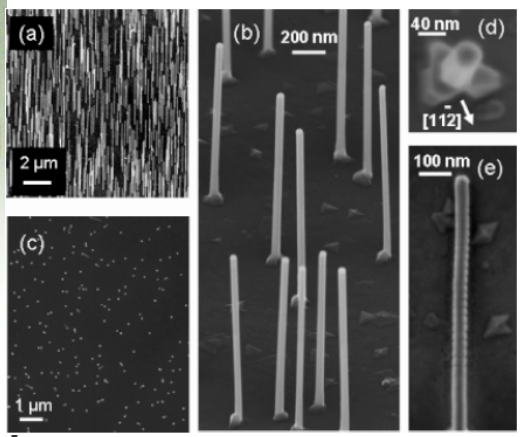
WP3: NANOWIRE PHYSICS & CHARACTERIZATION
- Transport and optical studies of InAs & InP NWs
- X-ray diffraction studies of discrete & arrays of III-V NWs
- Tight-binding modelling of heterostructures and doping

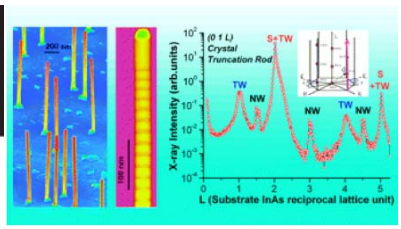
NANO LETTERS
2007
Vol. 7, No. 9
2596−2601

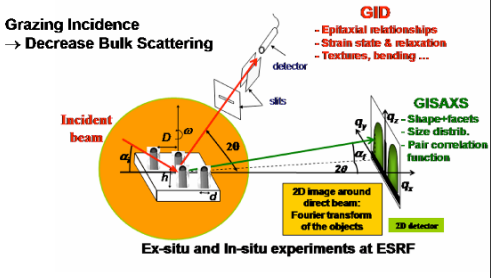
Strain and Shape of Epitaxial InAs/InP Nanowire Superlattice Measured by Grazing Incidence X-ray Techniques

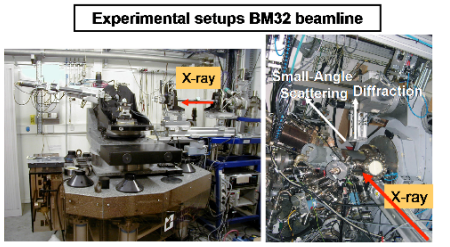
Joël Eymery,* François Rieutord, Vincent Favre-Nicolin, Odile Robach, Yann-Michel Niquet, Linus Fröberg, Thomas Mårtensson, and Lars Samuelson

CEA Grenoble, Département de Recherche Fondamentale sur la Matière Condensée, Service des Matériaux et Microstructures, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France, and Solid State Physics, Lund University, Box 118, S-221 00 Lund, Sweden









Ex-situ GIXR goniometer
Equipped with furnace.

In-situ GIXR goniometer (UHV)
Effusion cells (CBE soon)

Work performed during the 2nd year:

WP1: NANOWIRE GROWTH
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- Studies of NW-dielectric interfaces
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- Transport and optical studies of InAs & InP NWs
- X-ray diffraction studies of discrete & arrays of III-V NWs
- Tight-binding modelling of heterostructures and doping

WP4: NANOWIRE DEVICES
- Development of wrap-gate transistors in InAs and Si NWs
- Realization and bench-marking of state-of-the-art NW FETs
- Lateral Si NW Schottky-barrier FETs demonstrated

small 2007, 3, No. 2, 230 – 234

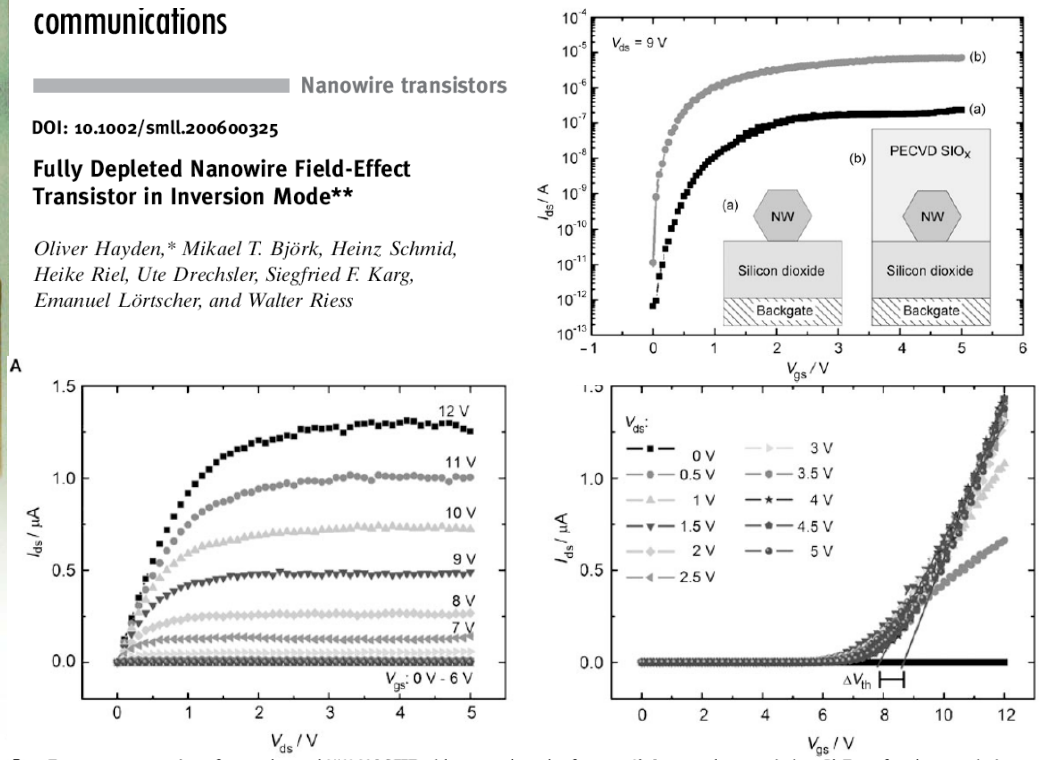
communications

Nanowire transistors

DOI: 10.1002/smll.200600325

Fully Depleted Nanowire Field-Effect Transistor in Inversion Mode**

Oliver Hayden, Mikael T. Björk, Heinz Schmid, Heike Riel, Ute Drechsler, Siegfried F. Karg, Emanuel Lörtscher, and Walter Riess*

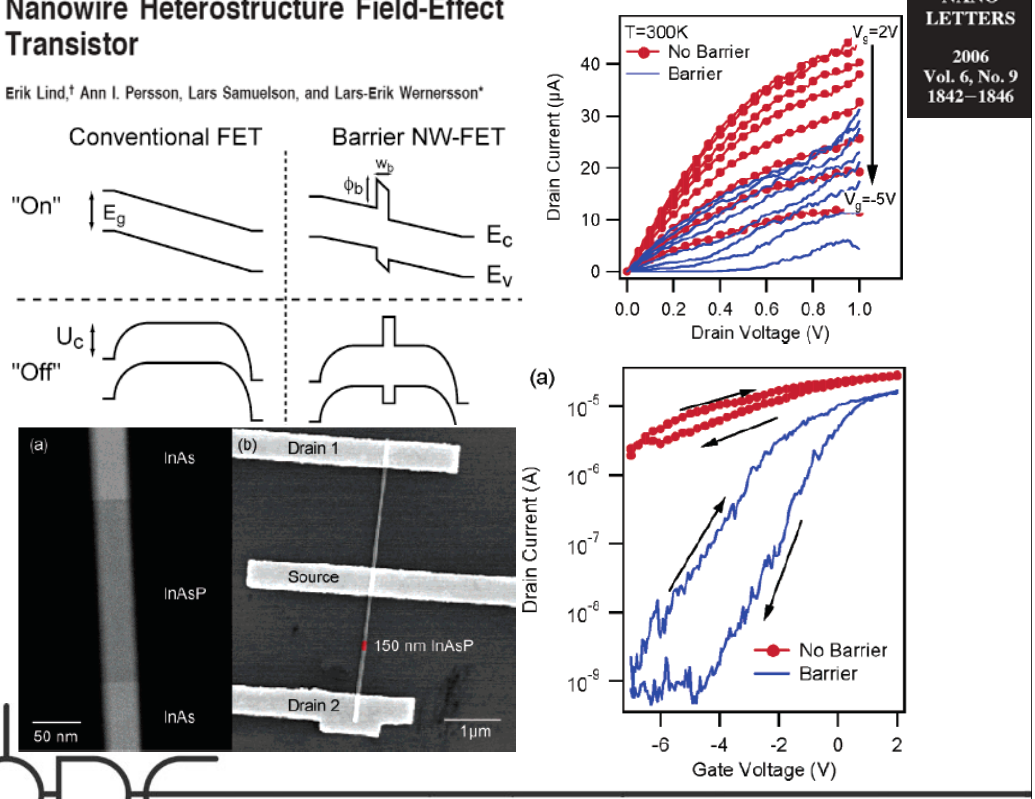


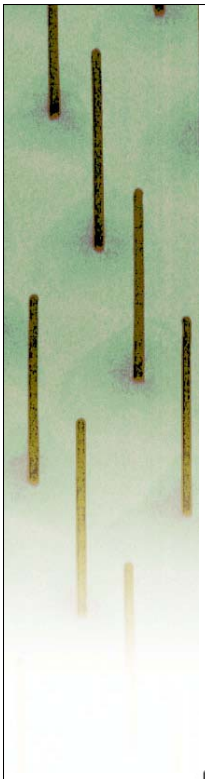
Transport properties of an n-channel NW MOSFET with a gate length of 2 µm. A) Output characteristics. B) Transfer characteristics

Improved Subthreshold Slope in an InAs Nanowire Heterostructure Field-Effect Transistor

Erik Lind,† Ann I. Persson, Lars Samuelson, and Lars-Erik Wernersson*

NANO LETTERS
2006
Vol. 6, No. 9
1842–1846





Work performed during the 2nd year:

WP1: NANOWIRE GROWTH
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WP2: NANOPROCESSING
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- Realization and bench-marking of state-of-the-art NW FETs
- Lateral Si NW Schottky-barrier FETs demonstrated

WP5: EVALUATION & INTEGRATION
- Vertical NW-based device concepts & architectures studied
- Implementation of NW-devices in silicon technology

WP6: INNOVATION-RELATED ACTIVITIES AND TRAINING
- Annual open NW symposia held in 2005, 2006 & 2007
- The public and internal website was maintained

NODE Review, Las Palmas, 15-16 November 2007

ICON 2007 Second International Conference on One-dimensional Nanomaterials
Malmö, Sweden, 26 – 29 September, 2007

2nd International Conference on One-dimensional Nanomaterials

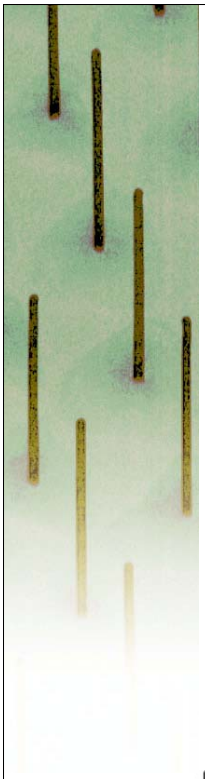
Malmö, Sweden, 26-29 September 2007
www.pronano.se/~icon

Conference Chairs: **Lars Samuelson** & **Reine Wallenberg**
Program Chair: **Knut Deppert**

Mildred Dresselhaus	*MIT*	**Paul Alivisatos**	*UC Berkeley*
Kenji Hiruma	*Hokkaido University*	**Mark Reed**	*Yale Univ.*
Brian Korgel	*Univ. of Texas, Austin*	**Zhong Lin Wang**	*Georgia Tech, Atlanta*
Li-Chyong Chen	*National Taiwan Univ.*	**Eleanor Campbell**	*Chalmers/Edinburgh*
Heike Riel	*IBM Rüschlikon*	**Rod Ruoff**	*Northwestern Univ.*
Mark Lundstrom	*Purdue Univ.*	**Heiner Linke**	*Univ. of Oregon*
Franz Josef Tegude	*Univ. Duisburg-Essen*	**Valéry Zwiller**	*TU Delft*
Carsten Ronning	*Univ. Göttingen*	**Mark Welland**	*Cambridge Univ.*
Magnus Borgström	*Philips Research*	**Jorg Appenzeller**	*IBM Yorktown Heights*
Bruno Chaudret	*CNRS Toulouse*	**Yann-Michel Niquet**	*CEA, Grenoble*

Co-sponsors: AVS, The Swedish Research Council, The Swedish Foundation for Strategic Research and the EU Project NODE
Organization: The Nanometer Structure Consortium at Lund University

SIXTH FRAMEWORK PROGRAMME



Papers published in refereed journals during year 2

1. "Nanowire-based one-dimensional electronics" Thelander et al. MATERIALS TODAY 9, 28 (2006)
2. "Position-controlled interconnected InAs nanowire networks" Dick et al. NANO LETTERS 6, 2842 (2006)
3. "Optimization of Au-assisted InAs NWs grown by MOVPE" Dick et al. J CRYSTAL GROWTH 297, 326 (2006)
4. "Phase segregation in AlInP shells on GaAs nanowires" Skold et al. NANO LETTERS 6, 2743 (2006)
5. "Nanowire-based multiple quantum dot memory" Nilsson et al. APPL PHYS LETTERS 89, 163101 (2006)
6. "Improved subthreshold slope in an InAs NW heterostructure FET" Lind et al. NANO LETT 6, 1842 (2006)
7. "Surface diffusion effects on growth of nanowires by chemical beam epitaxy" Persson et al. JAP 101, 1 (2007)
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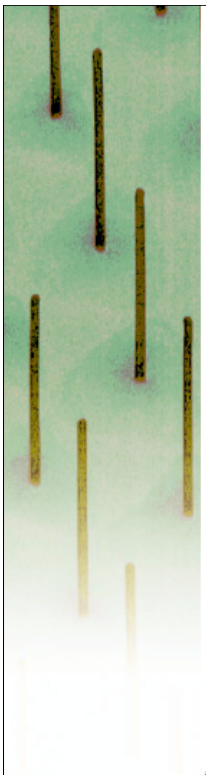

Status report:

We are in a very productive state of the work

We have mastered many of the critical growth, characterization & device processing challenges

We have reached state-of-the-art devices, but need to put stong efforts into integration issues

We have a vision for how NW-devices will form a basis for new circuit architectures/platforms

… and we have a lot of fun together!