

# Implementation of a microprocessor using a two-dimensional semiconductor

Stefan Wachter, Dmitry K. Polyushkin<sup>1</sup>, Ole Bethge<sup>2</sup>, Thomas Mueller<sup>1</sup>

<sup>1</sup>TU Wien, Institute of Photonics, Gusshausstraße 27-29, 1040 Vienna, Austria

<sup>2</sup>TU Wien, Institute of Solid State Electronics, Floragasse 7, 1040 Vienna, Austria

[stefan.wachter@tuwien.ac.at](mailto:stefan.wachter@tuwien.ac.at)

During the past decades, the invention and subsequent rise of the microprocessor has had a tremendous impact on society. While these devices so far are nearly exclusively made from silicon, continuously increasing demands regarding speed and integration density have prompted research into different materials as an alternative [1, 2]. Due to their immunity to short-channel effects, mechanical flexibility and improved electrostatic gate control semiconducting TMDs such as two-dimensional molybdenum disulfide show great promise [3].

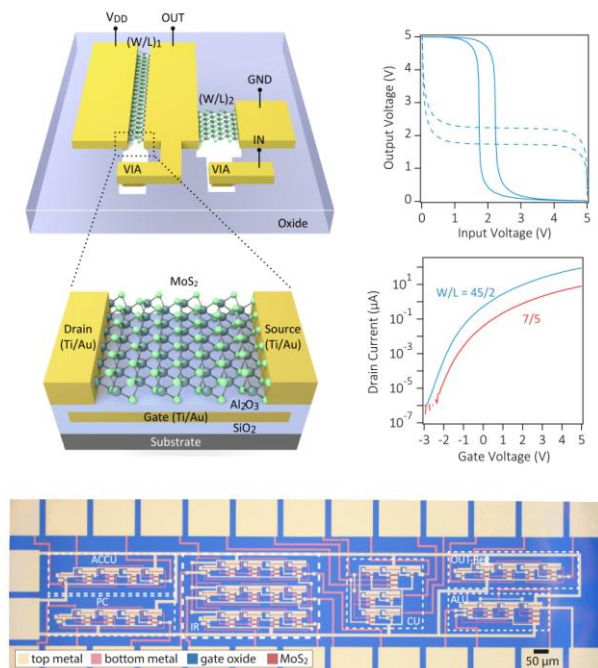
In our work [4], we demonstrate a single-bit implementation of a microprocessor using CVD-grown bilayer MoS<sub>2</sub>. Our processor is based on the NMOS logic family and consists of 115 transistors that form several registers used to store I/O-data, a program-counter to facilitate program flow, an ALU performing the actual operations and a control unit coordinating the function of the other subunits. It can run simple, user defined programs that consist of logical operations and are stored in an external memory.

Using careful design of the W/L ratios of our FETs we were able to cascade 14 stages of logic components. A short program of 10 instructions was executed, confirming correct rail-to-rail operation of our processor. It constitutes the most complex logic device using two-dimensional semiconductors fabricated to date [5] and is readily scalable to multi-bit data.

## References

- [1] M.M. Shulaker *et al.*, Nature 501, (2013) 526–530
- [2] K.F. Mak *et al.*, Phys. Rev. Lett. 105, (2010) 136805
- [3] G. Fiori *et al.*, Nature Nanotech. 9 (2014), 768–779
- [4] S. Wachter *et al.*, arXiv:1612.00965, (2016)
- [5] L. Yu, *et al.*, Nano Letters, 16 (2016), 6349–6356

## Figures



**Figure 1:** Schematic of an inverter circuit and an individual MoS<sub>2</sub>-transistor in gate-first technology (left) and measurement results of single transistors as well as inverters (right). The bottom shows an optical image of our microprocessor. Metal pads are used for testing, communications with periphery and wire-bonded together to realize internal connections.