Novel Logic and Memory Devices in Graphene

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Advances in graphene growth and device processing have enabled a host of advanced device concepts. We will describe field effect transistors (FETs) and beyond-CMOS ideas such as tunnel FETs which show negative differential resistance (NDR) that are enabled by the unique properties of graphene [1-2]. We will discuss applications of such devices in memory and logic circuits. Challenges in large scale integration of such devices and commercialization will be discussed.

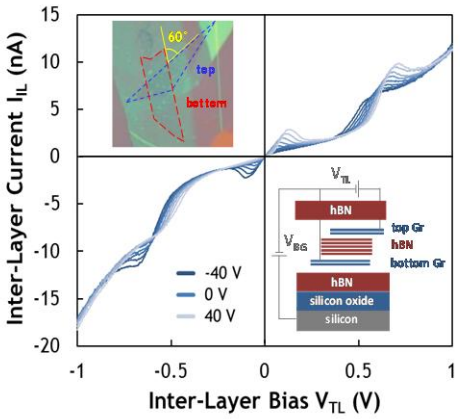

Figure 1: Bi-layer graphene-hBN tunnel FET showing negative differential resistance (NDR).

References:

1. B. Fallahazad, K. Lee, S. Kang, L. Register, S. Banerjee and E. Tutuc, Nano Letters (15) Issue: 1 (2015) Pg: 428-433

2. S. Kang, B. Fallahazad, K. Lee, H. Movva, K. Kim, L. Colombo, L. Register, E. Tutuc, S. Banerjee, IEEE Electron Device Letters, (36) Issue: 4 (2015) Pg: 405-407.

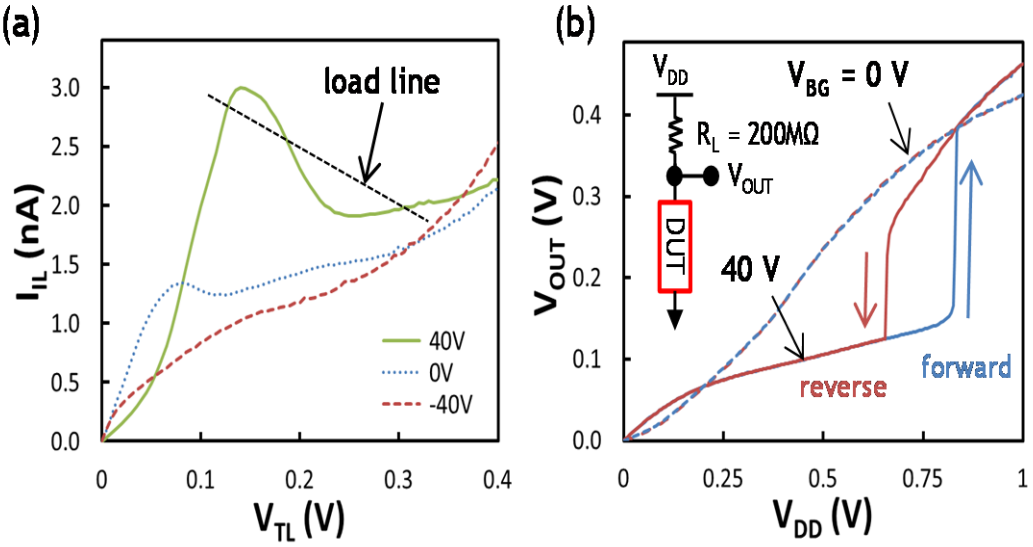

Figure 2: Use of NDR in 1-transistor static random access memory circuit. Conventional CMOS SRAMs require 4 transistors.