Large-signal model of graphene field-effect transistors

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Abstract

A circuit-compatible compact model of the intrinsic capacitances of graphene field-effect transistors (GFETs) is presented. The main novelty is that the model guarantees charge conservation using a Ward-Dutton's linear partition scheme, which is relevant for simulation of a number of circuits where this aspect is key. The intrinsic capacitance model can predict the bias dependence of small-signal parameters at high frequency operation. Together with a compact drain current model [1], a large-signal model of GFETs is developed combining both models as a tool for simulating the electrical behavior of graphene-based integrated circuits, dealing with the DC, transient behavior, and frequency response of the circuit. The drain current model is based on a drift-diffusion mechanism for the carrier transport coupled with an appropriate field-effect model. The intrinsic capacitance model consists of a 16-capacitance matrix including self-capacitances and transcapacitances of a four-terminal GFET (Fig. 1 provides with an illustrative example). The large-signal model has been implemented in Verilog-A, being compatible with conventional circuit simulators allowing for technology benchmarking, performance metrics prediction and design of circuits offering new functionalities. The intrinsic description of the devices serves as a starting point toward the complete GFET device model that could incorporate additional non-idealities. It has been embedded in a general purpose circuit simulator for circuit performance benchmarking. Specifically, we have simulated a high-frequency performance amplifier [2], together with other circuits that take advantage of the graphene ambipolarity, such as a frequency doubler [3] (see Fig. 2), a radio-frequency subharmonic mixer [4] and a multiplier phase detector [5]. A variety of simulations comprising DC, transient dynamics, Bode diagram, S-parameters, and power spectrum have been compared with experimental data to assess the validity of the model.

Acknowledgments

This work is supported by Ministerio de Economía y Competitividad (projects TEC2012-31330 and TEC2015-67462-C2-1-R) and the European Union (No. 604391, 7th FP Graphene Flagship).

References

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TABLE. INPUT PARAMETERS OF THE GFET UNDER TEST.

Input parameter	Value	Input parameter	Value
T	300 K	L	500 nm
μ	1300 cm^2/Vs	W	840 nm
V_{gs0}	-1.062 V	L_t	5 nm
V_{bs0}	0 V	L_b	300 nm
Δ	0.140 eV	ε_{top}	12
$\hbar\Omega$	0.075 eV	ε_{bottom}	3.9
R_s, R_d	1.1 kΩ·μm	R_g	20 Ω

Figures

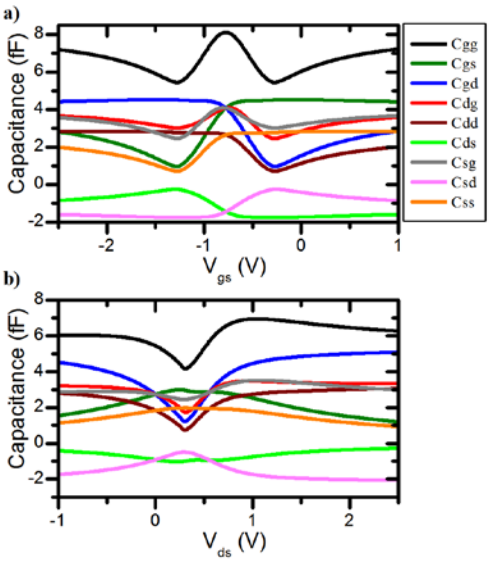

Fig. 1 Compact model calculation of selected independent intrinsic capacitances versus a) the gate bias (at V_{ds} = 1 V and V_{bs} = 40 V) and b) drain bias (at V_{gs} = -1 V and V_{bs} = 40 V) for the device described in the table.

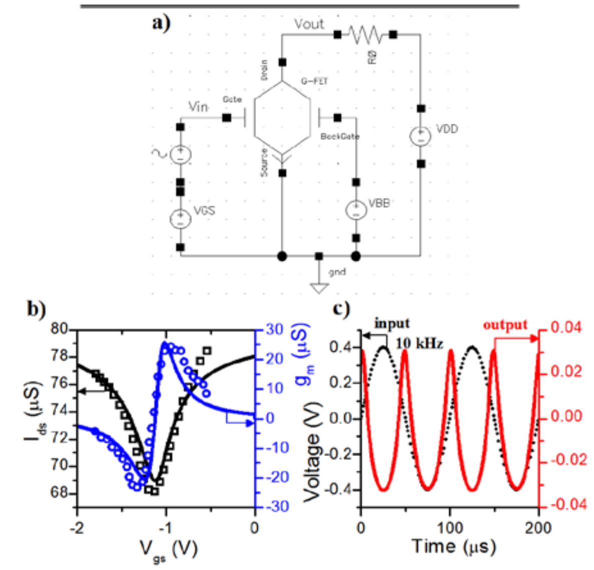

Fig. 2 a) Schematic circuit of the GFET based frequency doubler (R_0 = 10 kΩ). b) DC transfer characteristics and transconductance of the GFET described in the table (V_{DD} = 1 V, V_{BB} = 40 V). c) Input and output waveforms (f_{in} = 10 kHz; A = 0.4V; V_{GS} = -1.15 V)