The role of the Fermi level pinning in gate tunable graphene/semiconductor junctions: Barristor

Ferney A. Chaves* and David Jiménez
Departament d’Enginyeria Electrònica, Escola d’Enginyeria, Universitat Autònoma de Barcelona, Campus UAB, 08193 Bellaterra (Barcelona), Spain.

*ferneyalveiro.chaves@uab.cat

Abstract
Graphene based transistors relying on a conventional structure cannot switch properly because of the absence of an energy gap in graphene. To overcome this limitation, a barristor device (Fig. 1) was proposed by Yang et al. [1], whose operation is based on the modulation of the graphene/semiconductor Schottky barrier by means of a top gate. ON-OFF current ratio up to $10^5$ was demonstrated for a barristor. That large number is likely due to the realization of a clean interface with virtually no interface trapped charge that could spoil the barrier height tunability. However, it is indeed technologically relevant to know the impact that interface trapped charge might have on the barristor’s electrostatics and carrier transport. For such a purpose we have developed a physics based model of the gate tunable graphene/semiconductor heterostructure where non-idealities such as Fermi Level Pinning (FLP) have been considered. Our study suggests that the barristor is a feasible graphene logic device achieving high enough on/off current ratio. When FLP dominates the barristor's electrostatics, the gate electrode cannot modulate the SBH anymore and rectification could be totally lost (Fig. 2). On the other hand, our model has revealed that the barristor exhibits changes of the threshold voltage induced by the drain-source voltage, similarly to the Drain Induced Barrier Lowering in short channel MOSFETs. It turns out that the barristor has to be biased at low $V_{ds}$ to get a sufficient ON-OFF current ratio.

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