The CV Characteristic of H-intercalated Epitaxial Graphene/Al2O3 MOS Capacitors

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Abstract

The investigation of the Capacitance-Voltage (CV) characteristic of (H)ydrogen-intercalated epitaxial graphene is of fundamental importance for the development of Graphene Field Effect Transistors. Using CV, it is possible to gain insight into fundamental phenomena occurring in graphene MOS structures. CV measurements are performed from 77 K to 300 K on graphene-MOS structures in order to probe the temperature dependence of trapping phenomena in graphene.

H-intercalated epitaxial graphene is grown in a horizontal hot-wall CVD reactor at 1400 °C and is in-situ intercalated with Hydrogen at 800 °C on nominally on-axis chemo-mechanically polished 4H-SiC substrates. After graphene growth, MOS capacitor structures are fabricated on epitaxial graphene using standard semiconductor processing techniques. For the MOS structures, dielectric deposition is of particular importance. Dielectric deposition begins with the evaporation and thermal oxidation of 2 nm of Aluminum metal in two steps. The purpose of this initial step is to provide the necessary seed layer for Atomic Layer Deposition (ALD) of Aluminum Oxide on graphene [1]. Next, a thick 20 nm Al2O3 layer is grown via ALD. For the ALD growth Trimethyl-Aluminum is oxidized in an atmosphere of H20 at a temperature of 300 °C. Next, a second seed deposition and ALD layer is performed in order to build the field oxide to a final total thickness of ~50nm. The second growth stage is thought to be necessary to decrease the leakage via pinhole formation [2]. Identical MOS structures are also fabricated on lowly doped epitaxial SiC samples in order to serve as a control sample.

CV measurements are made on an Agilent E4980A LCR meter at 100 kHz in a tabletop Liquid Nitrogen cryostat. Figure 1 shows the CV data taken as a function of temperature. At low temperature, the CV data has a capacitance minimum near 0 V corresponding to the expected minimum in the density of states associated with the Dirac point in graphene [3,4,5]. As the temperature is increased, the Dirac cone becomes obscured due to the existence of traps in the oxide. Similar behavior is observed in the conductance curve. CV measurements made on SiC reference samples confirm the trapping of negative charge in the Alumina with accumulation bias as shown by the CV curve shifting to the right in consecutive measurements (Figure 3). Such behaviour is expected in Al2O3 which is not annealed at above 700 °C [6], and optimal performance of ALD films is achieved by annealing at 1000 °C for several hours [7]. There is initially no significant negative charge in the Alumina (the curve starts to go towards accumulation already at zero volts). In successive measurements, electrons are irreversibly injected into the oxide.

An analogous case of charge injection is observed in the graphene measurements. For appreciable positive bias, electrons are injected into the alumina from the graphene. As these electrons are trapped one expects a shift of the Dirac point to higher bias. Such a shift was observed occasionally in graphene MOS structures. Since there is no significant flatband shift in the Al2O3/SiC structures we would expect that the Dirac point is not significantly shifted in Al2O3/graphene samples at negative bias [7]. Thus, the CV data the SiC and the graphene are phenomenologically correlated. The data indicates that the ALD Al2O3 is of poor quality. From the accumulation capacitance on the SiC samples, the dielectrc constant of the ALD Al2O3 may be perhaps underestimated at ε_r=3.0. Regardless, this is substantially lower than the expected value of 8-10. Current research is directed towards the improvement of the ALD by annealing at high temperature. It remains to be see what effect of high temperature annealing has on H-intercalated graphene layers.

References

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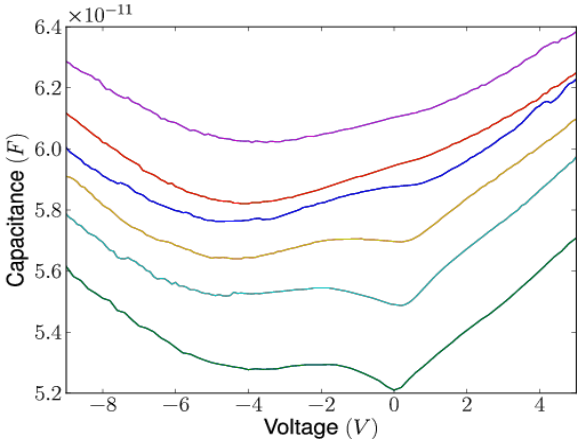


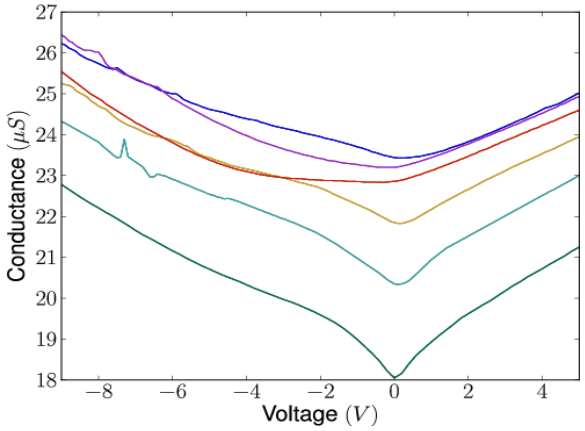
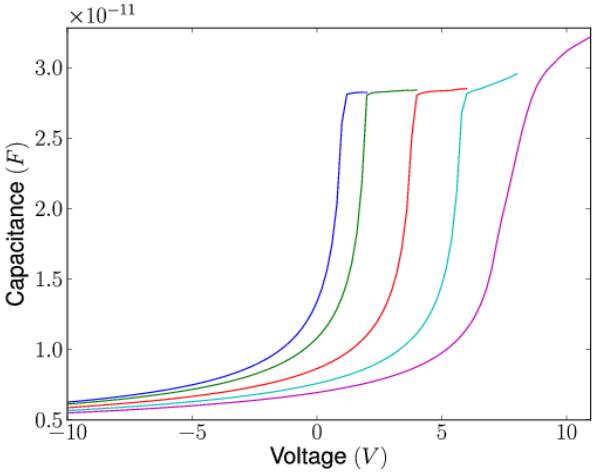


Figure 1 (left): CV measurements taken as a function of temperature from 77 K (green) to 300 K (red). At 77 K a capacitance minimum is observed around 0V indicating the existence of a Dirac Cone. The capacitance is measured on a MOS structure with a circular pad of diameter 400 μm.

Figure 2 (right): Complementary GV measurements to those shown in Figure 1. A conductance minimum is observed near 0 V at all but the highest temperatures. The high conductance values indicate high leakage through the ALD oxide layer.



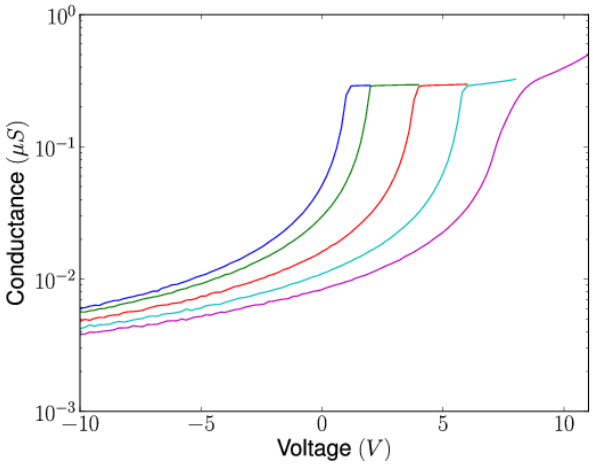


Figure 3 (left): CV measurements on SiC reference samples taken at 77 K. Accumulation is visible near 10 V positive bias. The movement to the right of each successive sweep indicates the filling of deep traps within the Al2O3. Measurements are taken at 100 kHz.

Figure 4 (right): Complementary GV curves to those shown in Figure 3. The conductance is observed to increase rapidly as the MOS structure is pushed into accumulation because of leakage through the oxide.