Tunable, Ultralow-Power Switching in Memristive Devices Enabled by Graphene-Oxide Heterogeneous Interface

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The application of graphene in electronics has been a widely anticipated yet very challenging goal. Especially, the lack of bandgap hinders its use as logic transistors. On the other hand, graphene has a unique property that the Fermi energy can be tuned in a wide range due to low density of states (DOS) near the Dirac points. When forming heterostructures with other materials, the interfacial barrier height can be tuned by gating, leading to many novel devices such as tunneling transistors with high on/off ratio, barristors, and photodetectors. One of the intrinsic limitations of these heterogeneous devices is the low drive current, partly due to the low DOS of graphene that inhibits efficient carrier injection. This is unfavorable for high-performance logic transistors, but could be favorable in information storage, where low energy operation (reading and writing) is attractive.

In this talk, we will present our recent works on the resistive memory applications of graphene heterostructures.[1] We integrate large-area CVD graphene into TiO_x-based memristive devices to realize ultralow switching power and non-linear I-V characteristics simultaneously. Compared to conventional Pt-based memristive devices (PtMD), graphene-based ones (GMD) show a significant switching power reduction up to ~880 times. In addition, GMD do not sacrifice other merits such as memory window, endurance and retention. We find that the interface between graphene and TiO_x plays a dominant role in device switching and therefore offers a unique playground to engineer memory characteristics. Such tunability can be realized by the quality and Fermi energy of graphene, which is not possible in conventional metal/oxide/metal structures. Finally, flexible and transparent GMD are demonstrated on Poly(ethylene naphthalate) (PEN) and show excellent retention against mechanical bending. The extra-low switching current down to 1μA and high resistance in our GMD is especially interesting in computing applications, such as neuromorphic applications, where huge parallelism requires very low leakage currents and thus high device resistance.

References

[1] Min Qian, Yiming Pan, Fengyuan Liu, Miao Wang, Haoliang Shen, Daowei He, Baigeng Wang, Yi Shi *, Feng Miao* and Xinran Wang*, "Tunable, Ultralow-Power Switching in Memristive Devices Enabled by Graphene-Oxide Heterogeneous Interface", Adv. Mat., in press (2014).

Figures

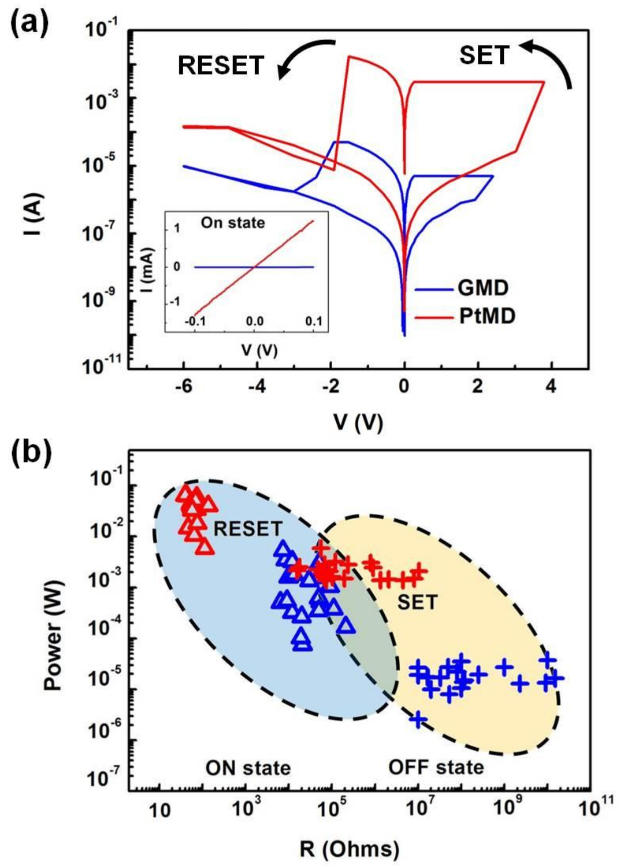

Figure caption: (a) Switching curves of a typical GMD (blue) and PtMD (red) with 5µA and 3mA SET current compliance respectively. The arrows point to the switching directions. Inset shows small bias I-V curves for both devices at ON state, showing significantly different resistance. (b) Resistance versus switching power of 20 different GMD and PtMD. Triangles denote R_{ON} and the corresponding P_{RESET}, while crosses denote R_{OFF} and the corresponding P_{SET}. Blue: GMD; red: PtMD.