Statistical Study on the Variation of Device Performance in CVD-grown Graphene FETs

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Abstract

Following the recent discovery of graphene [1], its field-effect mobility as high as 15000 $cm^2/V.s$ and a Fermi velocity of ~10^8 cm/s have been demonstrated at room temperature [2]. These intriguing physical properties of graphene have accelerated rapid research activities for exploring its electronic properties further, most of which are yet to be unraveled. In this paper, we report a statistical study on the variation of performances observed from measurements of CVD-grown Graphene FETs (GFET) on different dies fabricated using identical process steps, reflecting on the process quality of Graphene layer as well as ohmic contact formations. The GFETs under study were characterized in several different dies using both current-voltage and S-parameter measurements under identical biasing conditions for the GFET gate width of 12 µm and oxide thickness of 3 nm. The typical gate length used is 300 nm. The typical I_D-V_{DS} and I_D-V_{GS} are shown in Figure 1 depicting both measurement and simulation [3] results. The scalable electrical compact model developed in [3] is used here, which shows fair agreement with the measurement results. In Figure 2 (a), S parameters of a typical device after de-embedding are shown as a function of the frequency. The small signal model used to extract the parameters from the S-parameter measurements is shown to fit the experimental results in Figure 2(a). The magnitude of the current gain (H21) from both simulation and measurements are shown in Figure 2 (b) for three different samples on the same die with identical dimensions, depicting three different cut-off frequencies. Figure 3 illustrates the statistics on variation of On-current (Figure 3 (a)), and Dirac voltage (Figure 3 (b)) in the same die (D6). Figure 3 (c) shows the Dirac voltage as a function of the applied drain-source bias. The peak cut off frequencies obtained after de-embedding of S-parameters are shown in Figure 4 (a) for different devices on different dies. The results show a wide range of variation even in the same die. Similar statistics on the variation of other small-signal parameters (g_m, g_{ds}, C_{gs}, C_{gd}, R_{gs}, R_{gd} and R_{ds}) are shown in Figure 4 (b)-(d) as extracted from the de-embedded S-parameters. Note that, the C_{ds} capacitance extraction, in most of the devices, showed a very small value of about 1 aF. The variations observed for different parameters among the wide range of devices measured in different dies of the CVD-GFET reflect on the fact that even with identical dimensions and biasing conditions, the process quality of the Graphene transfer may play a major role in determining device performance despite good interface quality (as also indicated by negligible gate current in the devices). Also, as extracted from our measurement results, the drain-source access resistances may vary widely due to poor contact formation with the graphene (high contact resistances), resulting in fluctuation of device parameters. Thus, we can infer some new directives towards the possible future of Graphene-electronics regarding good quality of contacts with the Graphene as well as quality of the Graphene channel for future high-performance GFETs.

References

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[2] A. K. Geim and K. S. Novoselov, *Nature Materials*, **6** (2007) pp. 183.
[3] S. Fregonese, M. Magallo, C. Maneux, H. Happy, and T. Zimmer, *IEEE Trans. Nanotechnology*, **12** (2013), pp. 539-546.

Figures

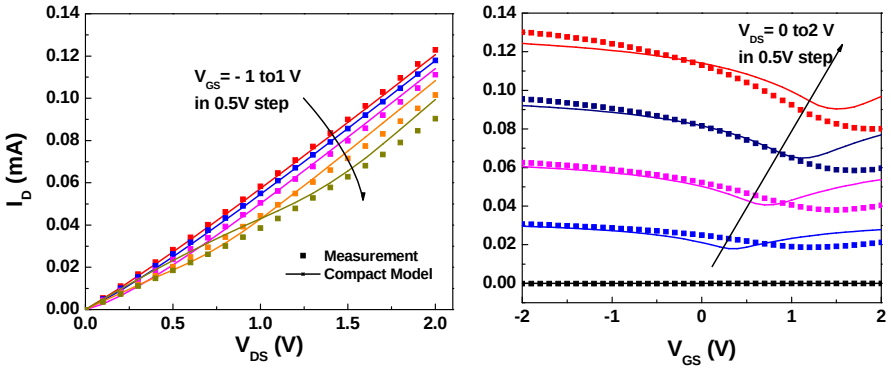

Figure 1: Typical I_D-V_{DS} and I_D-V_{GS} characteristics of the GFET under study.

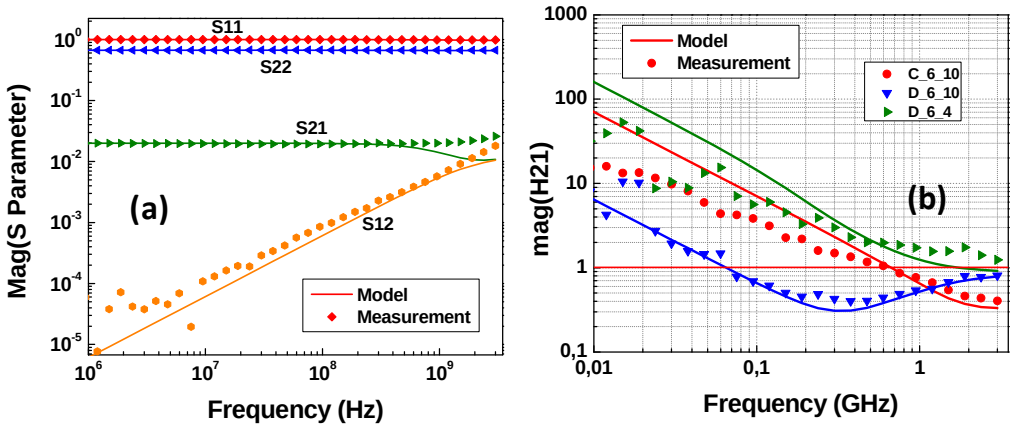

Figure 2: (a) Typical GFET S-parameters after de-embedding, (b) Magnitude of H21 for three GFETs.

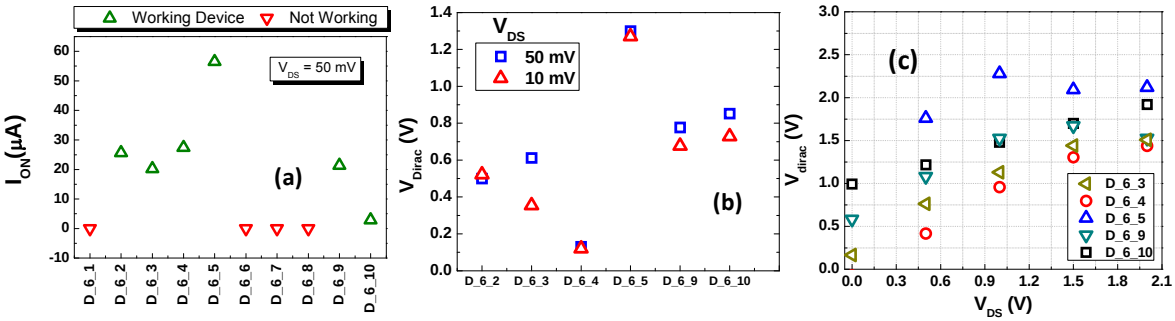

Figure 3: Statistics on the variation of (a) On-current, (b) Dirac voltage for the CVD GFETs on the same die (D6) for identical dimensions and biasing conditions, and (c) Dirac voltage as a function of V_{DS}.

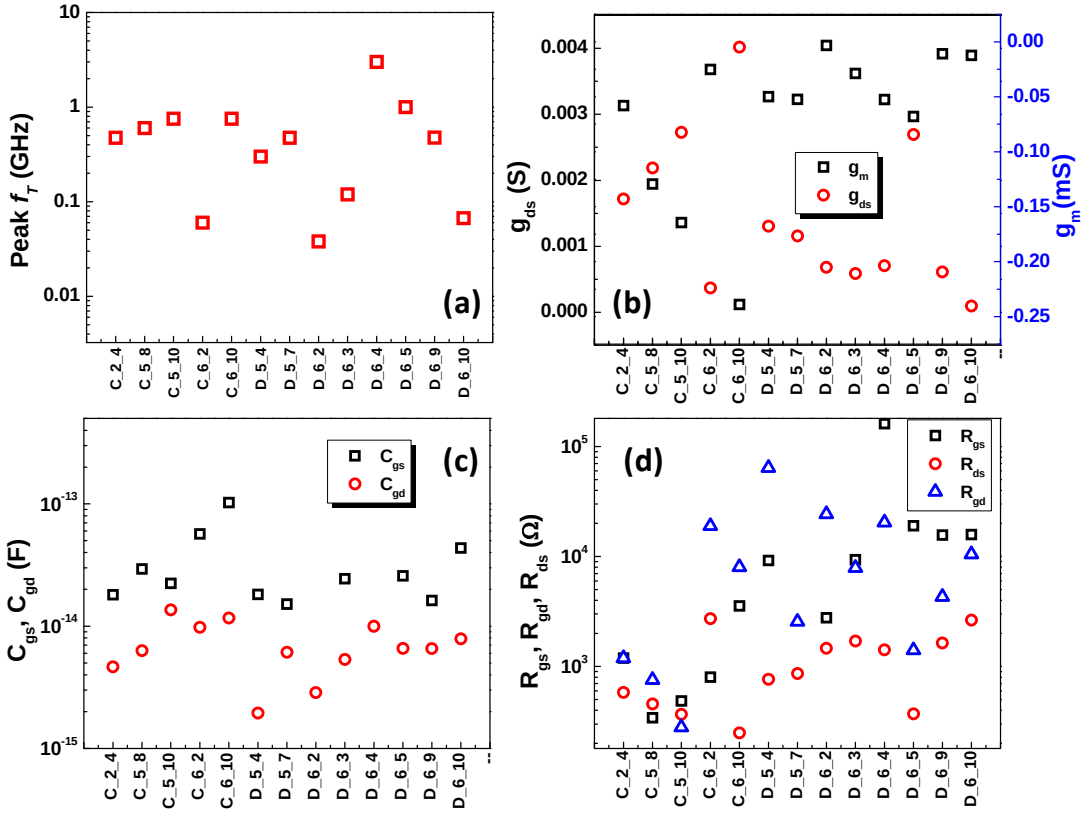

Figure 4: Statistics of the variation of (a) peak cut-off frequency, (b) transconductance (g_m, g_{ds}), (c) gate-source and gate-drain capacitances and (d) gate-source, gate-drain and drain-source resistances as extracted from the de-embedded S-parameters of the CVD-GFETs.