Challenges in integrating graphene into CMOS technology platform

Grzegorz Lupina, Andre Wolff, Mindaugas Lukosius, Julia Kitzmann, Gunther Lippert, David Kaiser, Jarek Dabrowski, Chafik Meliani, Christian Wenger, Ioan Costina, Markus Andreas Schubert, Wolfgang Mehr

IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
lupina@ihp-microelectronics.com

Abstract

Graphene and graphene-based devices have a great potential to considerably extend the use and functionality of Si CMOS technology [1,2]. Graphene-enhanced modules (e.g. RF communication, optoelectronic, sensing) with superior performance improving the interaction with the user and the outside world can find application in many branches such as consumer electronics, automotive electronics, medical applications etc. Combination of the graphene-enabled non-digital functionalities with the digital CMOS world on one chip will require integration of this new material into the existing Si platform [2].

Here, we describe the results of first graphene integration trials into a professional Si wafer fabrication line located in a class-1 cleanroom and point out to challenges which should be addressed in the future. We have developed a graphene device fabrication scheme which can be used to manufacture a wide range of graphene devices such as transistors, sensors, or optoelectronic components. To demonstrate feasibility of the process in our initial experiments we focus on the realization of graphene base transistors [3,4]. We use commercially available CVD graphene which is transferred from Cu onto target 8-inch wafers. Fabrication begins with the preparation of patterned substrates (Fig. 1a) equipped with doped Si emitter areas (E) and metal contacts (M). Directly before graphene deposition, the substrate is etched to remove surface oxides and enable formation of graphene-Si Schottky emitter junction and ohmic metal-graphene contacts. Chip-size graphene layers (~20 mm^2) are placed on the prepared wafers (Fig. 1b) using wet transfer techniques. This process is scalable to larger graphene layer sizes. Transfer of graphene is followed by the deposition and patterning (photolithography, dry-etching, Fig. 1c) of the collector stack comprised of a high-k insulator (e.g. HfO_2) [5] or a semiconductor layer (e.g. Si) [6] and a metal contact layer C (Fig. 1d). In this way the structure of the vertical graphene base transistor is realized [3,7,8]. The terminals of the transistor are connected to Al signal-ground-signal measurement pads (Fig. 1e,f) using tungsten vias (Fig. 1g). Electrical characterization of the fabricated devices indicates that monolayer graphene preserves its characteristics even after many steps of harsh technological processing showing sheet resistance of about 2kOhm/sq. Well performing graphene-Si Schottky diodes and graphene/high-k/metal capacitor stacks are demonstrated. Among the challenges ahead is the reduction of graphene-metal contact resistance as well as finding solution to the problems associated with graphene transfer. The latter include well known inevitable cracks, folds and polymer residuals but also a considerable amount of Cu contamination which may be dangerous in CMOS fabrication lines. This underlines the need for a CMOS-compatible method enabling direct graphene growth on arbitrary dielectric and semiconducting substrates. Our attempts to achieve this challenging goal will be also presented here [9,10].

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Figure 1

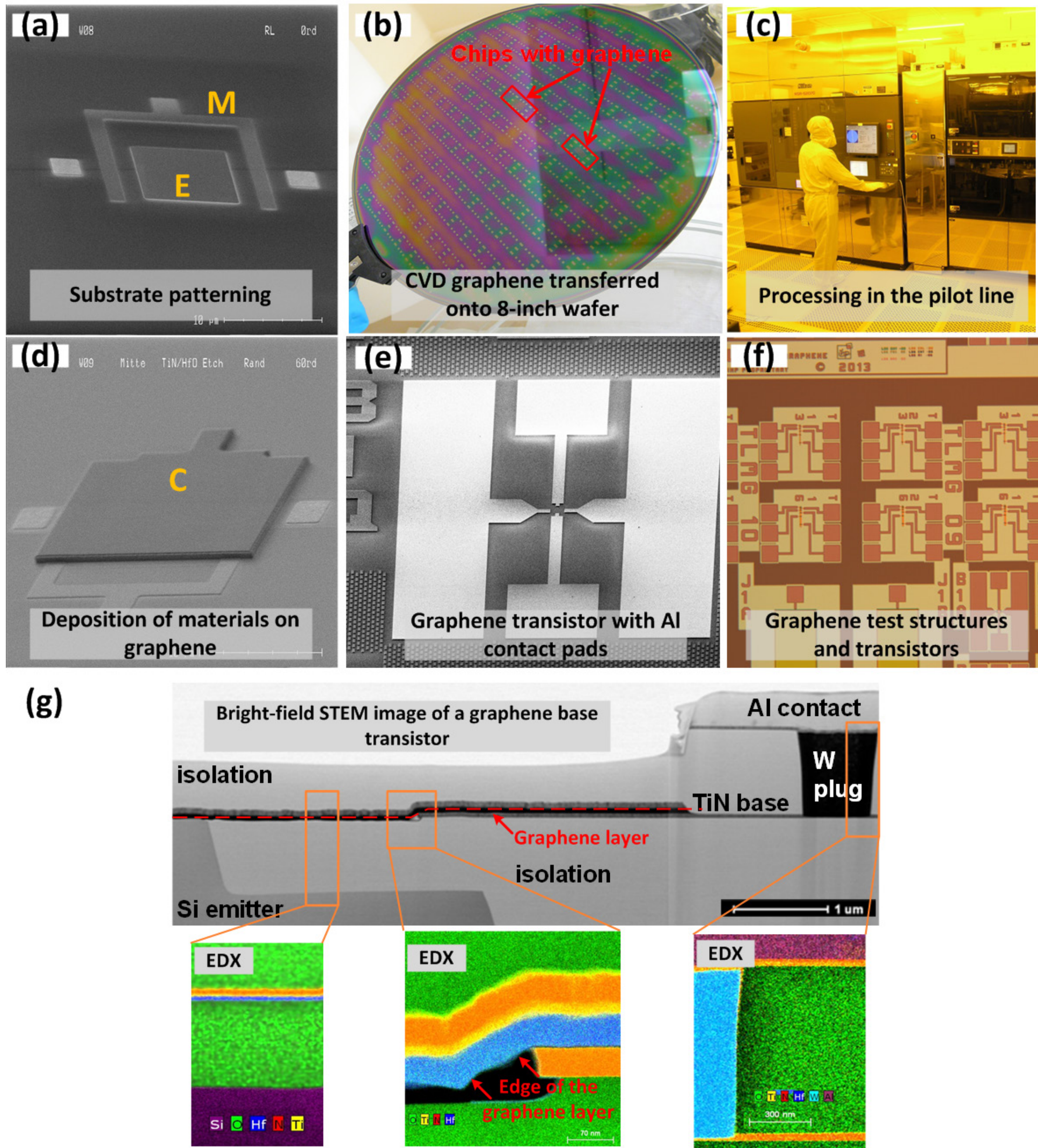

Fig. 1 Fabrication of graphene devices in a 8-inch Si wafer pilot line. (a) Preparation of patterned substrates. (b) Graphene transfer. (c) Processing in the pilot line. (d) graphene base transistor with collector high-k/metal stack deposited on graphene and patterned. (e-f) fabricated transistors and test structures. (g) STEM-EDX investigation of a graphene device fabricated using only Si technology compatible materials and processes