Graphene Field Effect Transistors on SiC with T-Shaped Gate: Homogeneity and RF performance

M. S. Khenissa, D. Mele, M. M. Belhaj, I. Colambo, E. Pallecchi, D. Vignaud and H. Happy

Institute of Electronics Micro and Nanotechnologies, Avenue Henri Poincaré, Villeneuve d’Ascq, France
ms.khenissa@ed.univ-lille1.fr

Abstract

Due to its very high carrier mobility, carrier saturation velocity, large critical current density [1-3], and the ultrathin body allowing channel length scaling without the non-ideal short channel effect [4-5], graphene has attracted enormous attention in recent years for radiofrequency transistor applications for post-silicon electronics [6]. Here we present field effect transistors (FETs) fabricated on a 1/4 of 2-inch graphene wafer where the homogeneity of the GFETS realized across the whole substrate was studied. Epitaxial graphene is synthesized on semi-insulating 4H-SiC wafers by thermal decomposition. The graphene is grown in a UHV chamber on the Si-face of the substrate at 1150°C under a Si flux. The number of layers and the quality of the graphene are characterized by Raman spectroscopy. As shown in figure (1), the characteristic Raman spectrum of graphene includes a narrow G-peak (1580 cm⁻¹) and a single Lorentzian 2D-peak (2685 cm⁻¹). The number of layers is estimated from the intensities ratio I_{2D}/I_G to be around 4 layers.

Structures for the Hall Effect Measurements were fabricated to measure the Hall mobility μ and the sheet carrier concentration n_s at 300°K in a Bridge configuration. The values of mobility and the sheet carrier concentration are respectively 780 cm²/Vs and 8.7 10^{12} cm⁻². The contact and sheet resistivity of the Ni/Au (10nm/40nm) stacking were determined by the Transmission Line Method. The values were extracted from the curve shown in figure 2, j = 2.1 x 10^5 Y/cm² and j_sn = 800 Y/sq.

We fabricated GFETs with a T-shaped gate to reduce the gate access resistance. The fabrication process flow is shown in the schematic diagram of figure (3-a). The graphene was patterned by e-beam lithography. The source and drain contacts of Ni/Au were obtained by e-beam evaporation metal deposition and standard lift-off. After the deposition of 2 nm of Al which was left to oxidize in air, 10 nm of Al₂O₃ were deposited by ALD at 300° C, to be used as a high k gate dielectric. We employed a standard trilayer resist E-beam lithography to realize T-shaped gates. Finally, coplanar accesses were realized. Figure (3-b) shows a scanning electron microscope (SEM) image of a full device and a cross section of a 170 nm T-shaped gate.

The devices were characterized both at DC and microwave frequency. The output characteristics of a graphene FET with L = 170 nm and W = 12 µm using are shown in figure (4) and the evolution of the transconductance g_ms is shown in figure (5). An output current of 25 mA as well as a transconductance of 2.6 mS are achieved at V_d = 2 V.

The RF performances of our GFET transistors were characterized by measuring S-parameters with a power network analyzer PNA (HP AGILENT 8510C) over the frequency range of 0.05 to 67 GHz under ambient conditions. The calibration of the measurement to the probe tips was performed by using LRRM calibration method. Based on our graphene layer, the typical bias condition for the gate electrode V_g = -3 V, and for the drain electrode V_d = 3 V since this condition provides g_m = 2.9 mS, as confirmed by DC measurement. Figure 6 presents both of the extrinsic (before de-embedding) and intrinsic (after de-embedding) current gain (H21) and maximum available gain (MAG) frequency response of the same graphene RF transistor measured on DC.

Figures 7 and 8 shows the number of the devices providing l and f_{max} in each range of frequency. We can remark that the majority of devices feature frequencies between 21 GHz and 34 GHz for l and between 12 GHz and 21 GHz for f_{max} reflecting the homogeneity of our graphene and technological process. An intrinsic cut-off frequency l as high as 43 GHz has been obtained and the maximum value of f_{max} is 23 GHz.

References

Figures

**Figure 1:** Raman spectra of Si-face few-layer graphene on SiC showing the G and 2D graphene peaks.

**Figure 2:** Resistance versus distance R(d) curve for a TLM structure.

**Figure 3 a)** process flow for GFET fabrication **b)** scanning electron microscope (SEM) image of a full device and a cross section of T-shaped gate

**Figure 4:** Output characteristics of a graphene FET with $L_g=180$ nm and $W=12$ µm

**Figure 5:** Number of devices in each range of $g_m$ transconductances, a value of 2.9 mS has been achieved.

**Figure 6:** GFET Current and power gain versus frequency for the device with $L_g=170$ nm and $W=12$ µm Bias point $V_{gs}=-3$ V, $V_{ds}=2$ V with $f_t=33$ GHz and $f_{max}=19.5$ GHz

**Figure 7:** Number of devices in each range of $f_{max}$ frequencies, a maximum oscillation frequency $f_{max}$ of 23 GHz has been obtained.

**Figure 8:** Number of devices in each range of $f$ frequencies, an intrinsic cut-off frequency $f_t$ of 43 GHz has been obtained.