Performance assessment of graphene-based lateral and vertical heterostructure FETs

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Abstract

Native graphene has a zero energy gap and it is therefore not suitable as a transistor channel material for digital electronics [1]. However, recent advances based on materials engineering have demonstrated graphene-based "*materials on demand*", with tailored properties [2,3]. *Vertical graphene heterostructures* have been proven to be suitable for FETs [4,5] and hot-electron transistors [6] exhibiting large current modulation [7].
Inspired by recent progress in the growth of seamless *lateral graphene heterostructures* [8-10], graphene-based lateral heterostructure (LH)-FETs have been proposed [11-13], exhibiting extremely promising switching behavior in terms of leakage current, propagation delay, and power-delay product. Despite the interest and the huge expectations of the research community shown towards these new devices, a comparative analysis of the performance against ITRS requirements for next-generation devices has never been done so far.
In this work, we explore the performance potential of state-of-the-art graphene based devices, which have already been demonstrated to provide large Ion/Ioff ratios. In particular, we will focus on the lateral heterostructure FET (LH-FET), and two FETs based on vertical graphene-based heterostructures: one proposed by Britnell et al. [4], that we call VH-FET, and the "barristor" proposed in [14]. The three device structures are shown in Figs. 1a-c. We do not consider transistors dedicated to analog RF applications [6].
Vertical Heterostructure FET Performance - We consider the VH-FET shown in Fig. 1b, experimentally demonstrated in [4-5] and also analyzed in [7]. The barrier consists of three atomic layers of boron-carbon-nitride, AB-stacked on graphene. Fig. 2a shows the pFET transfer characteristics for different valence band edge barriers BV. Performance figures shown are poor: the I_{on}/I_{off} ratio is always smaller than 20 and the delay time is four orders of magnitude larger than that expected from Internation Technology Roadmap for Semiconductors (ITRS) [15].
Barristor Performance - The device structure is shown in Fig. 1c. Silicon has a donor doping N_D and the gate dielectric has effective oxide thickness EOT. The gate voltage modulates the Schottky barrier between graphene and silicon exploiting the partial graphene screening properties. Fig. 3 shows that performance is again much worse as compared to ITRS requirements CMOS transistors, i.e. poor I_{on}/I_{off}, larger Power Delay Product (PDP) and intrinsic delay time (τ).
LH-FET Optimization and performance – Finally, we consider the double-gate p-channel LH-FET illustrated in Fig. 1a, BC_2N is lattice-matched to graphene and has a bandgap of 1.6 eV, offering a barrier to holes from graphene of 0.64 eV. As can be seen in Fig. 4a, the transfer characteristics are almost independent of t_B, and all performance parameters are optimized when $t_B = L$ (Figs. 4b). As can be seen, in this case, I_{on}/I_{off} is very large (10^4) and complying with ITRS requirements, outperforming VH-FET and the barristor device.
Conclusion - Finally, we compare in Fig. 5 the requirements of ITRS 2012 for high performance logic CMOS [12] with graphene-based heterostructure FETs. As can bee seen, LH-FETs exhibit lower intrinsic delay time and lower PDP than CMOS for the same gate length (considering 10 nm for 2020, and 7 nm for 2024). VH-FET and barristor cannot be included in the comparison since they exhibit larger delay times by at least four orders of magnitude. We are aware that our simulations do not consider the impact of dissipation in the channel, that typically reduces I_{on} by a factor of two. Even taking this aspect into account, graphene-based lateral heterostructure FETs stand out as the most promising graphene-based transistors for digital electronics.

References

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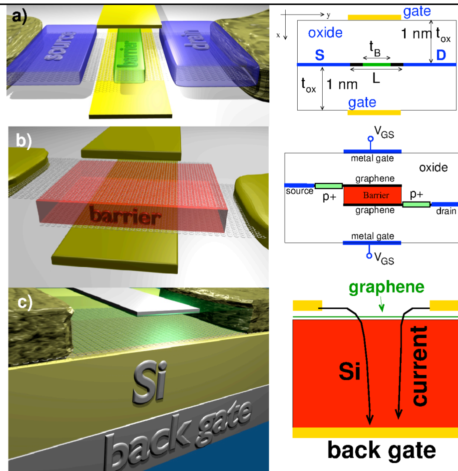

Figure 1: Device structure of a) LH-FET; b) VH-FET; c) Barristor.

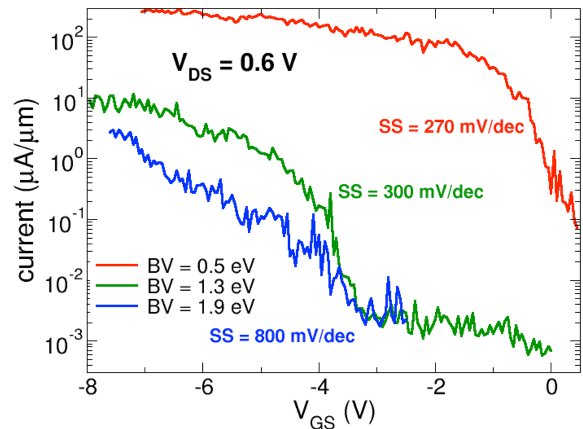

Figure 2: transfer characteristics of the VH-FET of Fig. 1b, for different values of the barrier BV at the valence band edge. The device has EOT = 0.62 nm (4nm HfO2), barrier thickness of three atomic layers

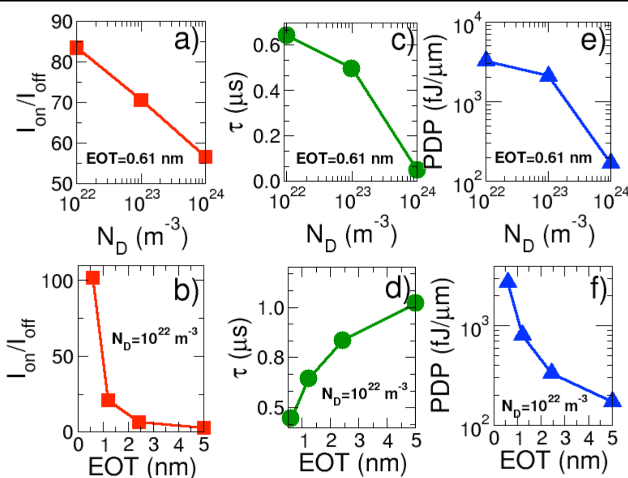

Figure 3: a) [b)] I_{on}/I_{off}, c) [d)] τ, and e) [f)] PDP of the barristor as a function of N_D for EOT = 0.61 nm [EOT for N_D = 10^{22} m^{-3}].

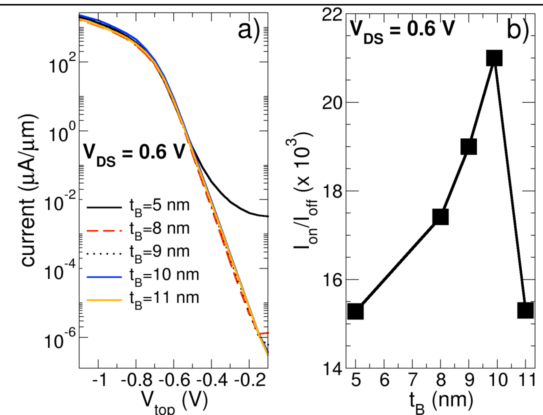

Figure 4: a) Transfer characteristics of the LH-FET for different values of tB. b) Ion/Ioff ratio as a function of tb. The device has the structure showninFig.1a,withL=10nm,tox =1nm,Vdd =0.6V,f=0.01.

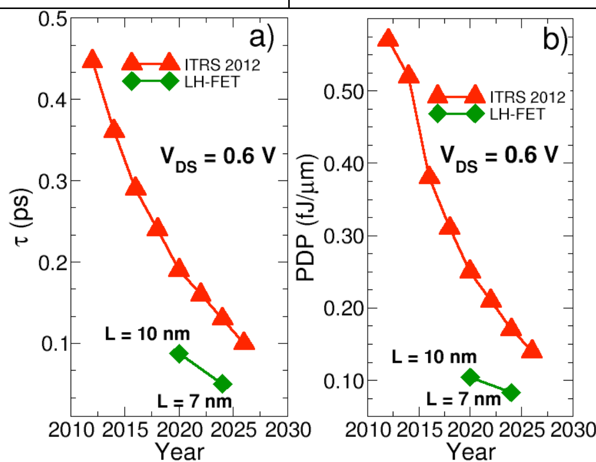

Figure 5: a) Intrinsic delay time τ and b) PDP as a function of year of shipment according to the ITRS 2012. On the same plot: comparison with simulation results for the LH-FETs with metal gate length of 10 nm (year 2020) and 7 nm (year 2024).