

Strategy of strain engineering to improve performance of graphene transistors

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Graphene, even with excellent transport properties, still has serious drawbacks for practical applications. In particular, its gapless character makes it difficult to turn off the current in graphene transistors and leads to a poor saturation of current. Many efforts of bandgap engineering have been made to overcome these limitations. For instance, they consist in cutting 2D graphene sheets into 1D nanoribbons [1], Bernal-stacking of graphene on hexagonal boron-nitride substrate [2], nitrogen-doped graphene [3], creating graphene nanohole lattice [4], and Bernal-stacking bilayer graphene [5]. However, each of these techniques still has its own issues.

Beyond expected applications in electronics, graphene also shows remarkable mechanical properties, i.e., it is amenable to a large strain of over 20% [6]. This suggests many possibilities of strain engineering to modulate the electronic properties of graphene and graphene nanostructures [7]. To open a bandgap in 2D graphene, a strain larger than $\sim 23\%$ is however required [8]. In this work, we consider the effect of uniaxial strain on the transport characteristics of the transistors based on unstrained/strained graphene junction. By means of numerical simulation, we will show that with only a moderate strain of 5%, the use of this strain hetero-channel can greatly improve the performance of graphene transistors.

Our calculations are based on the tight-binding model constructed in [8]. The strain causes the changes in the C-C bond vectors as $\vec{r}_{ij}(\sigma) = M_S(\sigma) \vec{r}_{ij}(0)$ where M_S is a diagonal matrix with $M_S^{11} = 1 + \nu\sigma$, $M_S^{22} = 1 - \nu\sigma$, σ is the strain and $\nu = 0.165$ is the Poisson ratio. The hopping parameters between nearest neighbor atoms are defined as $t_{ij} = t_0 \exp[-3.37 |r_{ij}(\sigma) - r_{ij}(0)|]$. This tight binding model is solved using the Green's function method, self-consistently with the Poisson's equation. The transport quantities are then determined after the self-consistency is obtained. The simulated devices are schematized in Fig. 1.

In Fig. 2, we first investigate the transport properties of graphene strain junctions. It is shown that a uniform strain does not change the gapless character of graphene. However, a significant conduction gap E_g opens in the strain junctions, i.e., $E_g \approx 360$ meV for the strain of 5% and can have a higher value for larger strain. Using this kind of strained junction, we demonstrate as displayed in Fig. 3 that the performance of graphene transistors can be significantly improved by a strain of a few %. In particular, a high ON/OFF ratio of over 10^5 can be obtained for a strain of 5%. Moreover, in the graphene tunneling device, the subthreshold swing can reach a value lower than 30 mV/dec. In the normal graphene transistors, the performance is additionally improved in terms of current saturation (with even a possible negative differential conductance, see Fig. 4) and hence high voltage gain is reached. Finally, we found as shown in Fig. 5 that the tunneling transistors exhibit interesting non-linear effects such as gate controllable negative differential conductance and strong current rectification.

In summary, we present an alternative approach to improve the performance of graphene transistors by using strain engineering. This type of strain engineering may be also useful for other devices based on graphene-like materials and for other applications.

References

- [1] M. Y. Han et al., Phys. Rev. Lett. **98**, 206805 (2007)
- [2] N. Kharche et al., Nano Lett. **11**, 5274 (2011)
- [3] A. Lherbier et al., Nano Lett. **13**, 1446 (2013)
- [4] J. Bai et al., Nat. Nanotechnol. **5**, 190 (2010)
- [5] Y. Zhang et al., Nature **459**, 820 (2009)
- [6] C. Lee et al., Science **321**, 385 (2008)
- [7] Y. Lu and J. Guo, Nano Res. **3**, 189 (2010)
- [8] V. M. Pereira et al., Phys. Rev. B **80**, 045401 (2009)

Figures

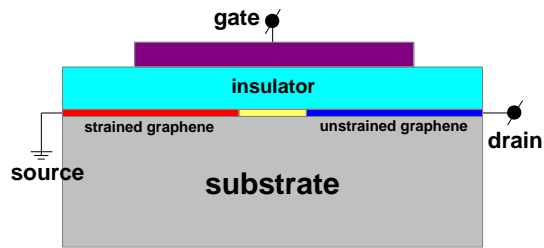


Fig. 1. Schematic view of simulated graphene transistors. The gate length is 80 nm and the length of the transition region (yellow zone) is 9 nm.

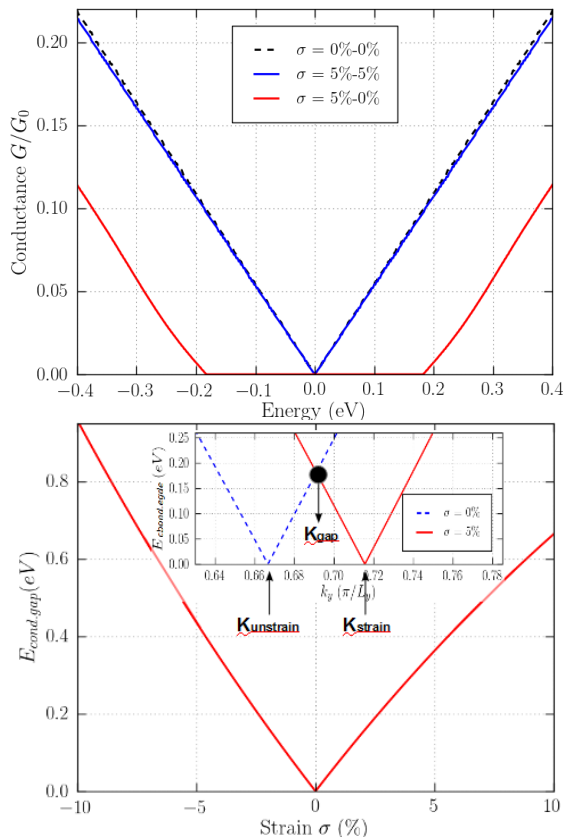


Fig. 2. Conductance as a function of energy (top) and conduction gap as a function of the strain (bottom) in strained/unstrained junctions.

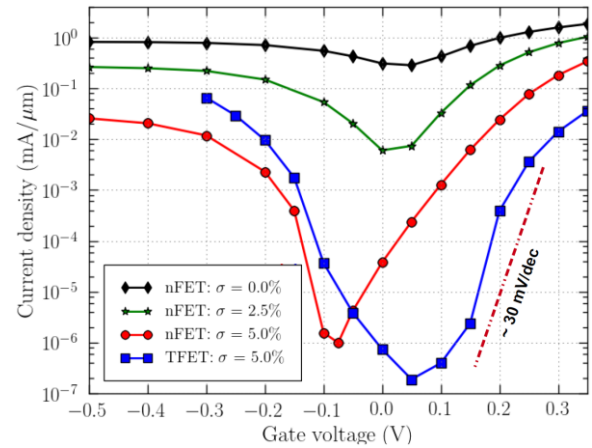


Fig. 3. Transfer characteristics of graphene FETs with different applied strains.

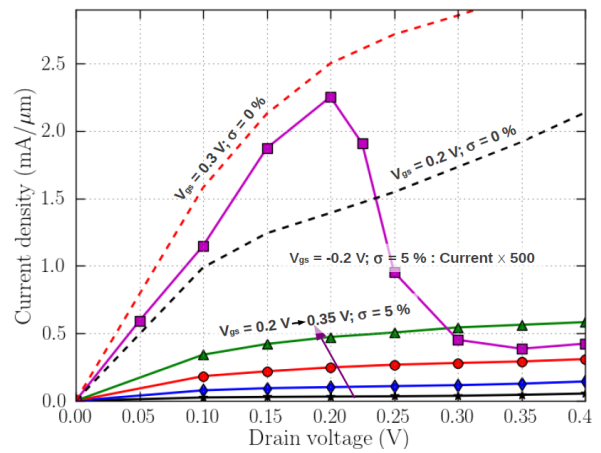


Fig. 4. I_D - V_{DS} characteristics of graphene FETs: strain junction ($\sigma = 5\%$) compared to unstrained case ($\sigma = 0$).

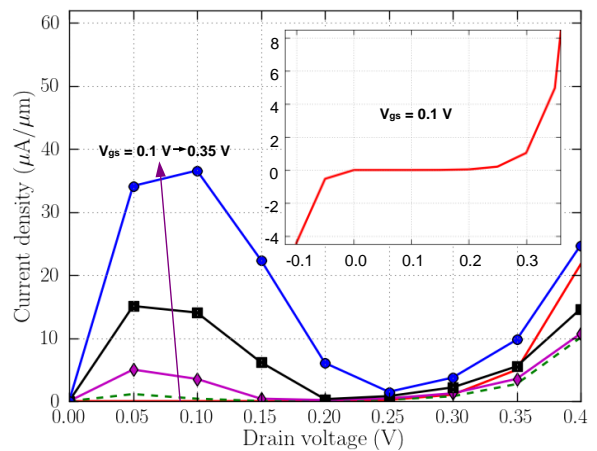


Fig. 5. I_D - V_{DS} characteristics of graphene tunneling FETs with $\sigma = 5\%$.