Modularity of CMOS-compatible synthesis of graphene by segregation methods Caroline Rabot^{1,*}, Alexandru Delamoreanu^{1,2}, Aziz Zenasni¹, Patrice Gergaud¹,

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The outstanding properties of graphene are expected to provide leads to a variety of technological challenges in microelectronics, alternative energies, health science, etc. One of the first expected commercial applications of graphene - where it could compete with actual materials due to its high transparency, conductivity, and flexibility (20% stretchable) - is the transparent electrode for photovoltaic devices, touch screens and light electroluminescent diodes. These applications require the development of graphene processes compatible with industrial implementation.

The present work emphasizes a simple and versatile route to grow graphene fully covering 200mm wafers in industrial-compatible equipments (Figure 1a). This route allows tuning the properties of graphene in term of topography, coverage, number of layers and defects using metals (Ni, Cu, Pt) and alloys. It is not limited to specific metals (even with very low carbon solubility) ; does not require any gaseous carbon source and can be performed at relatively low temperature (600-700°C). The whole process flow has been operated using standard semiconductor-compatible clean room facilities.

Using segregation behavior of carbon in metals [1, 2, 3], the solubility of carbon (from carbon-based source) in transition polycrystalline thin metal film (ex: nickel) leads to the formation of mono to few layers of graphene (Figure 1b). The resulting coverage is over 99% (fully interconnected) and highly uniform throughout all the 200mm wafer. Typical optical transmittance of ~80% at 550 nm and resistance of ~600-700 Ohm/sq have been obtained (Figure 2). This transmittance can be significantly improved with some additional treatments.

By tuning the materials chosen (Carbon-based materials and transition metal), different morphologies of graphene can be obtained (graphene on metals, graphene redeposited on the dielectric and suspended graphene) (Figure 1 c, d). All processes occur during the growth process itself on a metal thin film [4, 5]. Intermediate silicide phases are identified as a way to develop a large catalogue of graphene and offer new capabilities in the synthesis of large area of graphene at low temperature.

References

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Figures

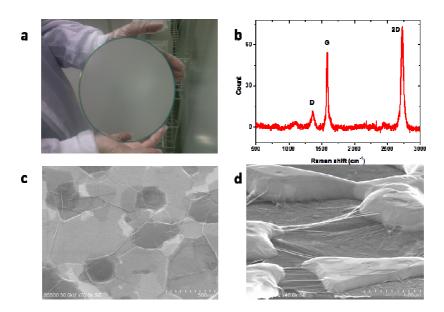


Figure 1: (a) Graphene synthesized on 200mm wafer. (b) Raman spectrum. (c-d) Scanning Electron microscopy images of graphene partially and fully suspended between Pt-based islands.

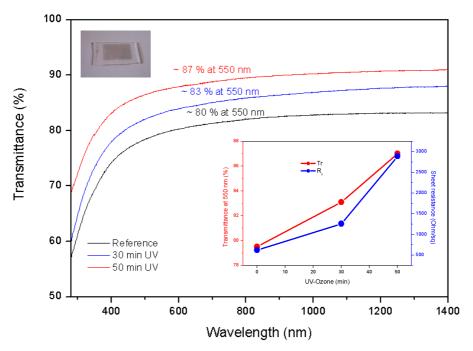


Figure 2 Transmittance spectra of graphene transferred on glass substrate without UV-Ozone treatment (black curve), with 30min UV-Ozone treatment (blue) and 50min treatment (red).