Nanoscale dual-gating of bilayer graphene on GaAs substrates

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The implementation of nanodevices into graphene has been an interesting but challenging topic. In particular, the lack of an energy gap is an obstacle for depleting carriers. A gap is at least required *locally* for gate defined devices out of a larger two-dimensional electron gas. An energy gap may be introduced by lateral confinement [1] or by breaking the inversion symmetry [2]. The former method leads to dimensions in the nm range which are hardly controllable lithographically and it causes large carrier-mobility degradation. Breaking the inversion symmetry, on the other hand, may be readily achievable in bilayer graphene [3] by applying an electric field perpendicular to the carbon atom planes (dual gating). However, a high sample quality over the dimensions of the gate metal is required to reduce the residual carrier concentration n_0 at the charge neutrality point. In this work we explore nanoscale dual-gating of bilayer graphene exfoliated on GaAs-substrates.

Exfoliation of bilayer graphene has been achieved on an insulating 300 nm thick GaAs-AlAs multilayer system [4]. The conducting GaAs substrate acts as back-gate. Top-gates have been fabricated using a sputtered layer of 17 nm thick Al_2O_3 as gate insulator on top of a thin Al precursor [5]. We will present measurements using large area top-gates to demonstrate that a high relative dielectric constant of about 8 as well as low-hysteresis performance has been achieved. A series of four 100 nm wide Ti-Au top-gates define an island of about 200 nm in diameter. The widths of the graphene flakes were at least 1 μm in all fabricated devices.

The diagram in Figure 1 shows the measured current I_{SD} through the device as function of bias voltage V_{SD} across the device. As the temperature is lowered from 4 K to 300 mK a transport gap opens without application of gate voltages. We employ finite element simulations to discuss the possibility of perpendicular electric fields resulting from the (grounded) top-gate metals straining the piezoelectric GaAs substrate. Variation of the back-gate voltage V_{BG} tunes the transport gap in an oscillatory fashion, as seen in Figure 2. The influence of the top-gates within the range of negligible leakage currents was limited. Therefore the current path through the island could not be unambiguously be verified. However, the oscillations indicate the formation of a localized transport path within the much wider graphene flake.

References

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[3] J. B. Oostinga *et al*., Nature Materials **7**, 151 (2008).
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Figures

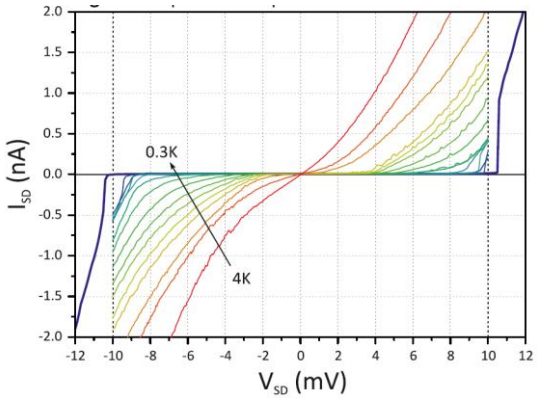

Figure 1: Temperature dependent I_{SD}-V_{SD} characteristic

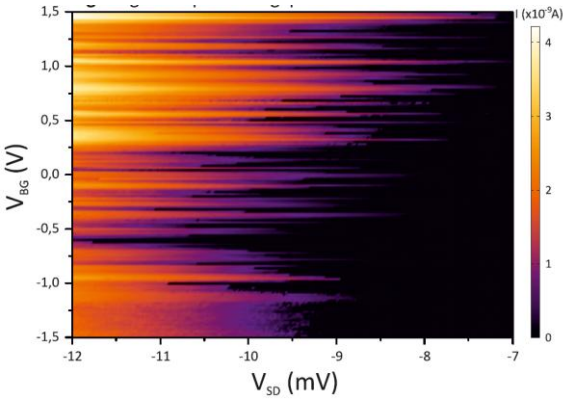

Figure 2: I_{SD}-V_{SD} characteristic for varying back-gate voltage V_{BG}