Tayloring the graphene/silicon carbide interface: a material system for monolithic wafer-scale electronics

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Graphene has many outstanding electronic properties and a vision of post-silicon electronics based on graphene is discussed. However, due to the absence of an electronic band gap transistors with high on/off ratio are still lacking[1]. Consequently, graphene circuits are currently limited to analogue amplification[2] and further modifications are needed for logic applications. Many efforts have been undertaken to establish a gap in graphene devices, with a band gap induced by bilayer graphene, spatial confinement, localization and chemical modification, resulting in rather small effects remote from technical requirements. For wafer based applications, we consider epitaxial graphene on silicon carbide (0001) as the first choice[3]. We propose a concept that monolithically employs the entire system epitaxial graphene, consisting of graphene, silicon carbide, and their common interface. For a transistor, graphene can be used as source, drain and gate electrode. The wide band gap semiconductor substrate silicon carbide forms the channel. Finally, two differently tailored interfaces introduce transistor functionality. The result is an epitaxial graphene transistor with high on/off ratio exceeding 10^4(see Fig. 1). Depending on the underlying substrate, both normally-on and normally-off operation is possible. The concept's particular strength is its capability for integration: within the same processing effort many epitaxial graphene transistors can be combined and complex circuits can be designed. In principle any logic functionality can be implemented.

References

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Figures

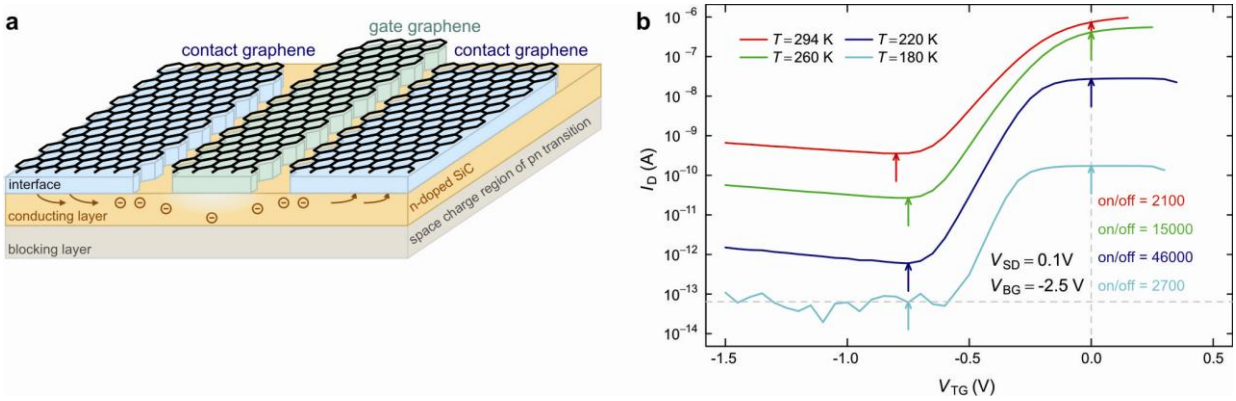

Figure 1
Figure 1a shows a scheme of our device. The graphene/silicon carbide interface is tailored in two different ways resulting in contact graphene *with ohmic contact to the semiconducting layer and* gate graphene *forming a Schottky contact. With these components we define a MeSFET-like transistor with silicon carbide as the semiconductor and graphene playing the role of both contact* and *gate metal.*
Figure 1b displays the transfer characteristics for various temperatures. On/off ratios were determined between V_{TG} = 0V and the minimum I_D value (indicated by arrows). The largest on/off contrast is achieved at T = 220 K. Improved surface quality, resulting in more homogeneous Schottky barriers, is expected to further reduce leakage currents and to extend high on/off performance to room temperature and beyond.