Graphene Crystal Growth and its Integration in Nanoelectronic Devices

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The semiconductor industry is facing major challenges in reducing the operating power in future integrated circuits. In the past decade, the state of the art Si-based electronics has gone from devices at or above 130 nm to the realm of 30 nm and below, with a defined pathway for logic and memory devices down to about 15 nm. As devices have scaled below a gate length of about 130 nm performance per power density has not scaled, in fact it has decreased.*(1)* As the semiconductor industry was evaluating approaches to address device power scaling through the evaluation of emerging materials and devices, graphene came into the scene and a number of devices based on graphene have been introduced and are now being developed, for example BiSFET devices*(2)*, various types of tunnel FETs, and p-n junction devices*(3)*. In addition to approaches trying to develop new low power switches, graphene for analog devices are also being developed; these devices do not require the stringent I_{on}/I_{off} ratios that logic devices do. The new devices have the potential for ultra-low power operation, high operating frequencies, and because of graphene's planar nature the films can be easily integrated in the conventional silicon flow.

In order to demonstrate any of the graphene based devices basic integration schemes, graphene films, dielectrics, metal contacts and electrodes will have to be selected and integrated without disturbing the basic transport properties of the graphene films. The effective fabrication of any device requires first identification and understanding of the specific device requirements to ensure that the appropriate level of effort can be dedicated to their development. There are many graphene applications and each has its own requirements, electronic devices have had the most stringent materials requirements to meet performance and reliability expectations and it will most likely be the same for graphene.

High quality graphene can be formed by exfoliation from natural graphite with samples sizes usually of a few hundred square microns. It has been shown that epitaxial graphene can also be grown on SiC substrates by a Si evaporation process from either the Si or C surfaces*(4)*. These films are limited to SiC substrates and are difficult to integrate on Si wafers. The successful demonstration and implementation of graphene-based device technology will require synthesis of high quality graphene large are films on substrates other than SiC or the exfoliation of graphene from graphite. The discovery of large-area and monolayer graphene growth on Cu substrates has certainly decreased the difficulty in procuring sufficient amount of graphene on arbitrary substrates for all types of graphene applications and specifically it has opened a major opportunity for transparent conductive electrodes for displays.*(5,6)* Further CVD graphene on Cu is enabling researchers and engineers to quickly make devices and establish repeatability that would otherwise be difficult to achieve. Growth of graphene on Cu by chemical vapor deposition (CVD) is unlike growth on other substrates such as Ni in that a self-limited monolayer of graphite is grown by a surface mediated process. In order to take full advantage of the fundamental properties of graphene and the synthesis of large area films it is necessary to grow uniform and nearly defect-free films as the semiconductor industry has done with silicon substrates.

The demonstration of a graphene-based devices will need high quality scaled dielectrics down to thicknesses of about monolayers as in the case of layers materials like hexagonal boron nitride, with a range of dielectric constants, $2 < K <$ high-k (> 20), and contacts with contact resistances of much less than 110 ohm-μm*(7)* achieved so far. Gate dielectrics on graphene have been deposited principally by atomic layer epitaxy (ALD) but since ALD is itself very surface sensitive, deposition of thin dielectrics on graphene proved extremely difficult. A number of nucleation techniques have been reported with some success including transfer of h-BN. However, uniform large area dielectrics with thicknesses less than about 2.5 nm are still not widespread.*(8)* A number of metals have been used as source and drain contacts but while reasonable devices have been fabricated low contact resistance similar to those achieved in silicon have not been achieved yet. But there are a few reports indicating that improvements can be made. In this presentation I will review the need for devices beyond CMOS, growth of large area graphene and integration of dielectrics and contacts with graphene and their effects on field effect transistors characteristics.

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