

Field-effect tunneling transistor based on vertical graphene heterostructures

L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist, A. K. Geim, K. S. Novoselov, L. A. Ponomarenko

School of Physics & Astronomy, University of Manchester, Manchester M13 9PL, UK
liambritnell@gmail.com

An obstacle to the use of graphene as an alternative to silicon electronics has been the absence of an energy gap between its conduction and valence bands, which makes it difficult to achieve low power dissipation in the OFF state. We report a bipolar field-effect transistor that exploits the low density of states in graphene and its one atomic layer thickness. Our prototype devices are graphene heterostructures [1,2] with atomically thin boron nitride or molybdenum disulfide acting as a vertical transport barrier. They exhibit room temperature switching ratios of ≈ 50 and $\approx 10,000$ respectively. Such devices have potential for high frequency operation and large-scale integration.

Our typical device vertical transistor architecture is as follows: we use graphene electrodes and a thin dielectric layer separating them in a vertical arrangement, with current flow perpendicular to the graphene's basal plane, figure 1. The two graphene electrodes are etched into Hall bar geometry so that we can measure the transport properties of the graphene leads, figure 2.

We are able to measure tunneling through the barrier—typically a few nanometers thick—by varying a bias voltage between the graphene electrodes. The application of a gate voltage dramatically alters the tunneling characteristics of the device, figure 3.

We explain the changes in the tunneling characteristics in our devices by a simple model [1,3] comprising three effects. (i) Movement of the Fermi level in both graphene electrodes (ii) movement of the relative position of their electronic bands and also (iii) lowering the effective barrier height. These combined effects result in a large increase in the leakage current between the graphene electrodes. The best device we have fabricated using hBN has a modest on/off ratio of ~ 50 and our first MoS₂ devices show a much improved ON/OFF ratio of $\sim 10^4$.

These devices are promising in development of the much vaunted application of graphene logic circuits, allowing minituration and high speed operation as the expected transition time for carriers is expected to be on the order of femtoseconds [4].

References

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Figures

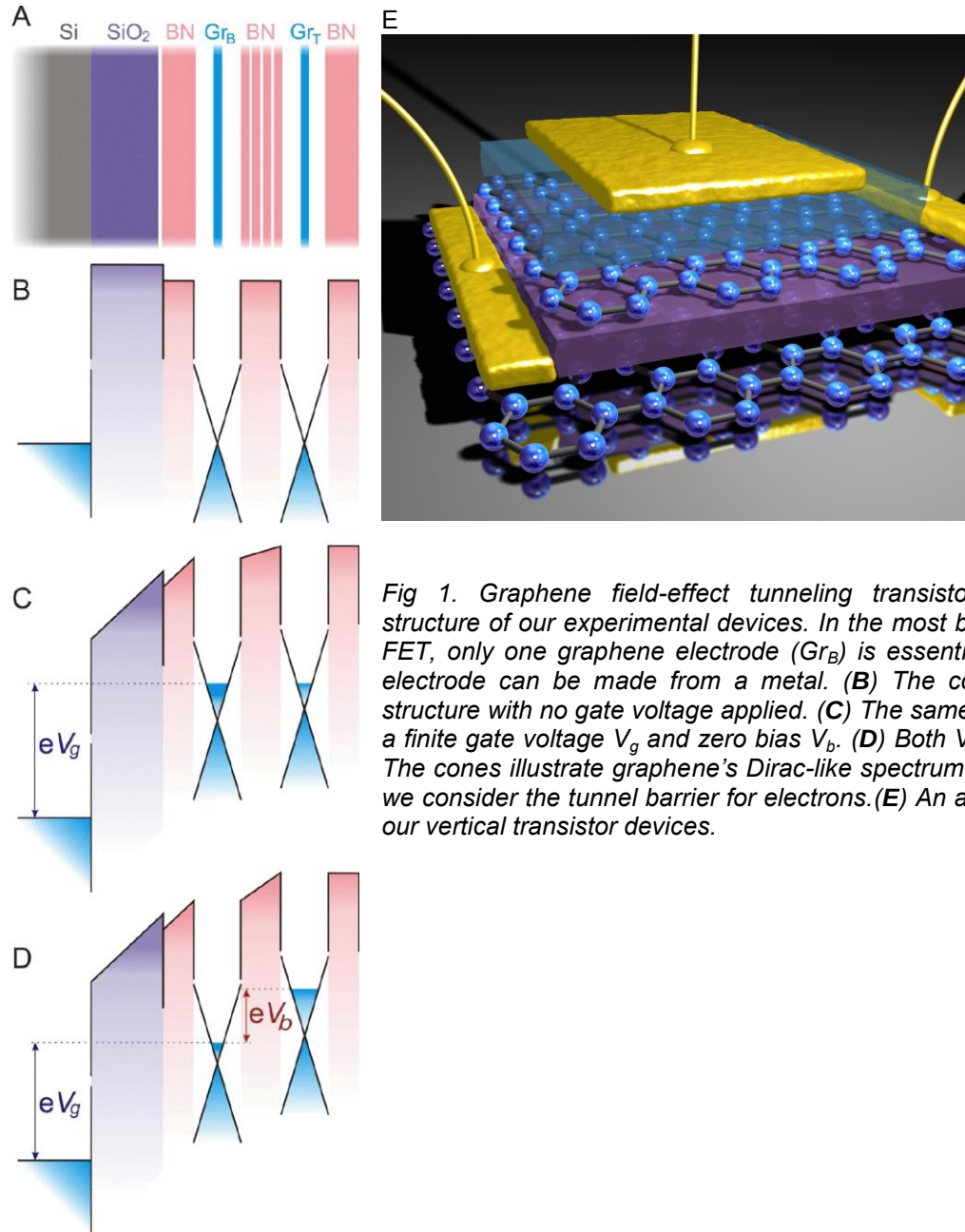


Fig 1. Graphene field-effect tunneling transistor. (A) Schematic structure of our experimental devices. In the most basic version of the FET, only one graphene electrode (Gr_B) is essential and the outside electrode can be made from a metal. (B) The corresponding band structure with no gate voltage applied. (C) The same band structure for a finite gate voltage V_g and zero bias V_b . (D) Both V_g and V_b are finite. The cones illustrate graphene's Dirac-like spectrum and, for simplicity, we consider the tunnel barrier for electrons. (E) An artistic schematic of our vertical transistor devices.

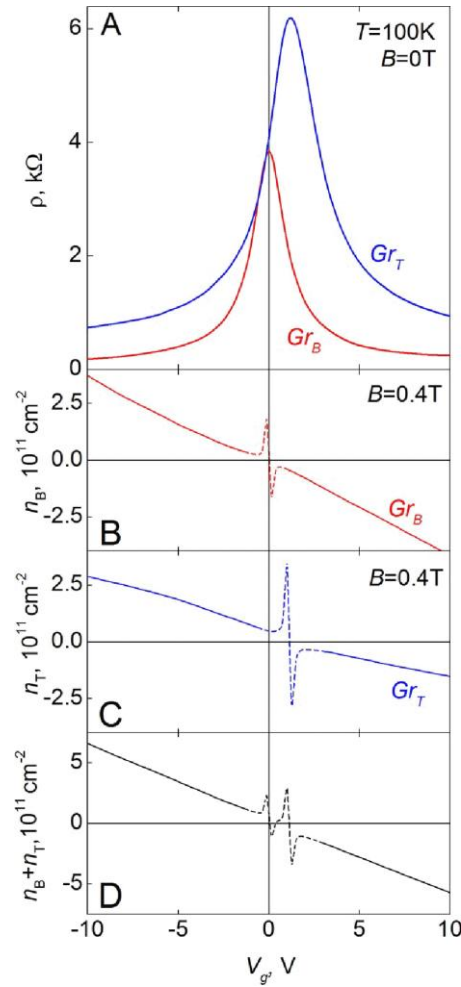


Fig 2. Graphene as a tunneling electrode. (A) Resistivities of the source and drain graphene layers as a function of V_g (B-D) Carrier concentrations in the two layers induced by gate voltage, which were calculated from the measured Hall resistivities. The shown device has a 4-layer hBN barrier.

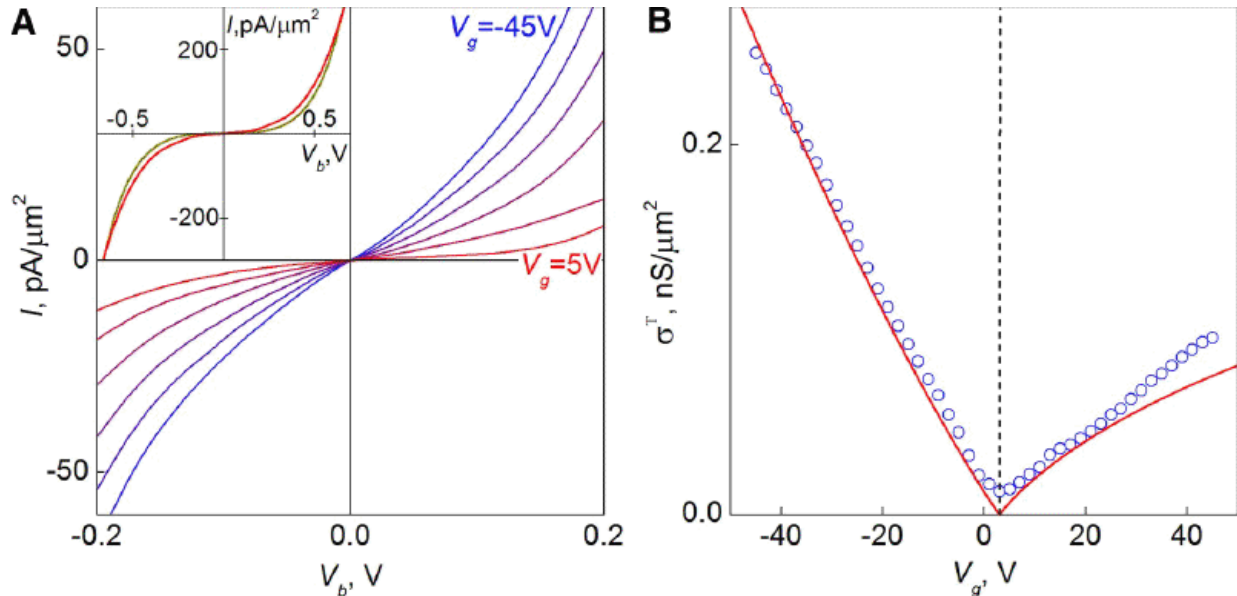


Fig 3. Tunneling characteristics for a graphene-hBN device with 6 ± 1 layers of hBN as the tunnel barrier. (A) I - V s for different V_g (in 10 V steps). Note, that due to the finite doping, the minimum tunneling conductivity is achieved at $V_g \approx 3V$. The inset compares the experimental I - V at $V_g = 5V$ (red curve) with theory (dark) which takes into account the linear DoS in the two graphene layers and assumes no momentum conservation. Further examples of experimental curves and their fitting can be found in Supporting online material of reference (). (B) Zero-bias conductivity as a function of V_g . The symbols are experimental data, and the solid curve is our modeling.