Valley FETs in graphene

Yu-Shu Wu, Mu-Kuen Lee, Maio-Ling Lin, Ning-Yuan Lue, and Yen-Chun Chen

National Tsing-Hua University, Hsin-Chu, Taiwan yswu@ee.nthu.edu.tw

Electrons in graphene exhibit the binary degree of freedom called valley pseudospin, due to the two-fold valley degeneracy at the Dirac points (K and K') in the graphene band structure. Protected by the large wave vector difference between K and K', the valley pseudospin has a sizable decoherence time allowing for the realization of the pseudospin-based electronics known as valleytronics.[1]. Previous theoretical works have developed a unified VOI-based methodology for the design of valleytronic devices. Such a methodology utilizes the VOI (valley-orbit interaction) that occurs between the pseudospin and an in-plane electric field and electrically manipulates the valley pseudospin to achieve device functions. Employing the methodology, a family of valleytronic devices including valley qubits [2], valley filters [2] and valley FETs [3] have been proposed. Here, for demonstration of the methodology, we consider the valley FET. The presentation will discuss its underlying principle and report our recent numerical simulation of electron transport through the structure based on the method of recursive Green's function.

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Wu et al., Phys. Rev. **B 84**, (2011), Chen et al., arXiv: **1605.**02250 [cond-mat.mes-hall].
Lee et al., Phys. Rev. **B 86** (2012), 165411; ibid **B 88** (2013), 125422.



Figure 1 The proposed valley FET - a Q1D channel in gapped graphene, with the source and drain being armchair nanoribbons and the channel defined and controlled by electrical gates.



Figure 2 Source / drain inject / detect electrons in the state $|K\rangle + |K'\rangle$. The channel pseudospin is rotated due to the VOI. Depending on the angle of rotation, the channel is on (for angle = $(2n+1)\pi$) or off (for angle = $2n\pi$)



Figure 3 Electron transmission vs. gate bias, for two channel widths.



Figure 4 Electron transmission vs. gate bias, for two channel lengths.